

High and Low side driver IC

FA5650N/51N

Application Note

6N1425b
6N1550

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Caution)

- The contents of this note will subject to change without notice due to improvement.
- The application examples or the components constants in this note are shown to help your design, and variation of components and service conditions are not taken into account. In using these components, a design with due consideration for these conditions shall be conducted.

1. Description

The FA5650N/FA5651N are high and low side driver IC, can drive Power MOSFETs and IGBTs that operate up to 800V. It composes elements of withstand voltage 5V/30V/800V in the same chip. Accordingly, it has built-in high and low side control/protection circuits, a level shift circuit of withstand voltage 800V and drivers of withstand voltage 30V.

When an HVIC(High Voltage IC) is used, a high side power device can be directly driven from a microcomputer or similar, optocoupler and pulse transformer become unnecessary and high-speed response is enabled. Therefore, downsizing and high reliability of the system can be secured.

2. Features

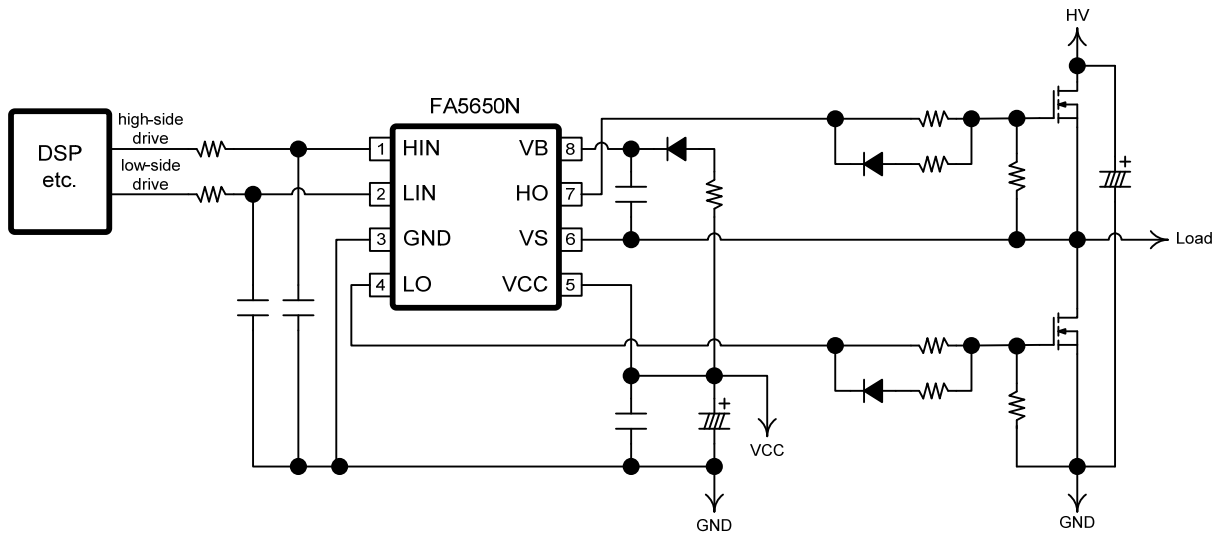
- High-side floating absolute voltage up to 800V
- High and Low side driver with 2 inputs and 2 outputs.
- 3.3V logic compatible
- Turn-on and turn-off propagation delay time typical 125ns
- Matched propagation delay below 30ns
- Undervoltage lockout for both channels
- Allowable offset supply voltage transient dVs/dt up to 50kV/us
- VCC and VBS supply range from 10V to 30V

Product Family

Type	High side power supply voltage to ground VB	Control power supply voltage VBS, VCC	Output current IHO, ILO	Package
FA5650N	830V	30V	-1.4A / 1.8A	SOP-8
FA5651N	830V	30V	-1.4A / 1.8A	SOP-16
FA5751N	624V	24V	-0.20A / 0.35A	SOP-8
FA5752N	624V	24V	High-side: -0.62A / 1.00A Low-side: -0.56A / 0.91A	SOP-8

3. Typical Connection

FA5650N



FA5651N

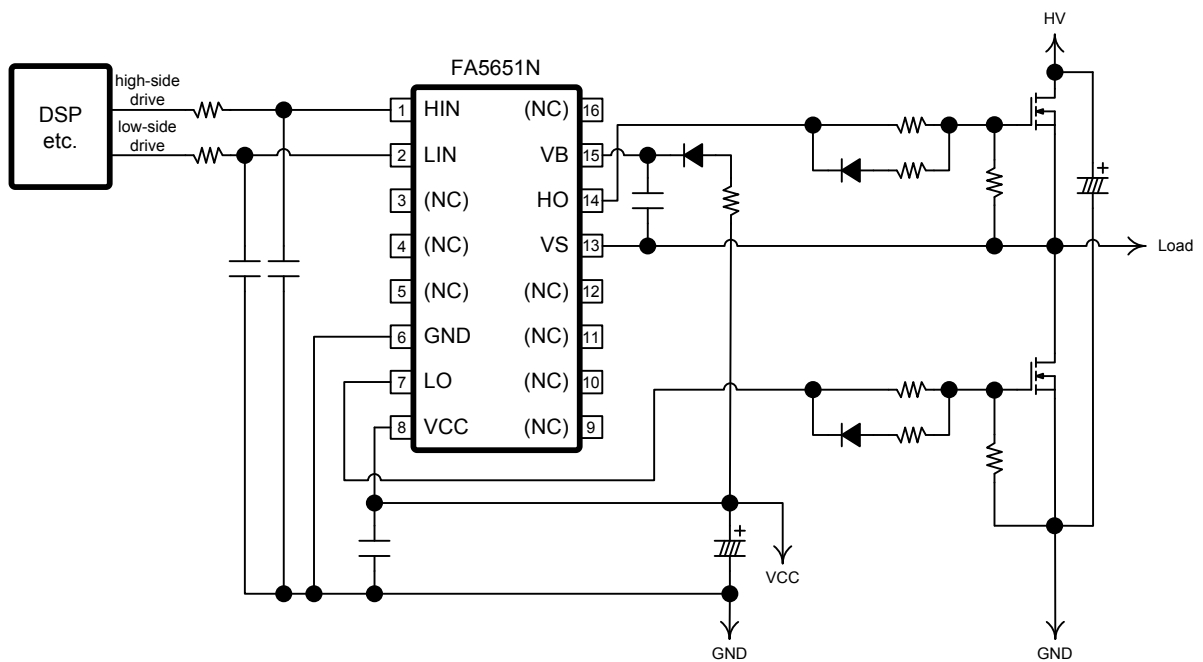


Figure 1. Typical Connection

4. Block Diagram

Internal circuit of FA5651N is the same as FA5650N.

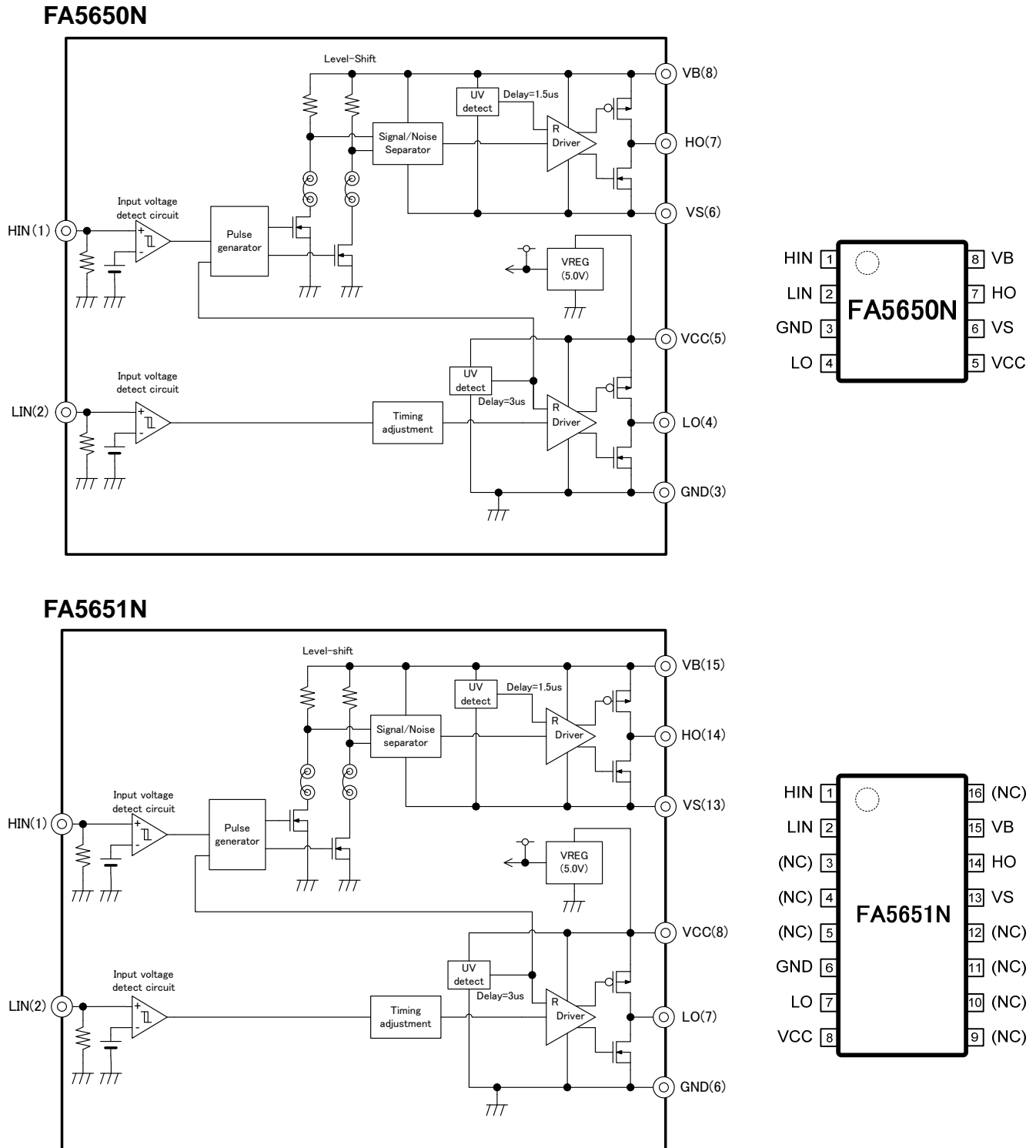


Figure 2. Block Diagram

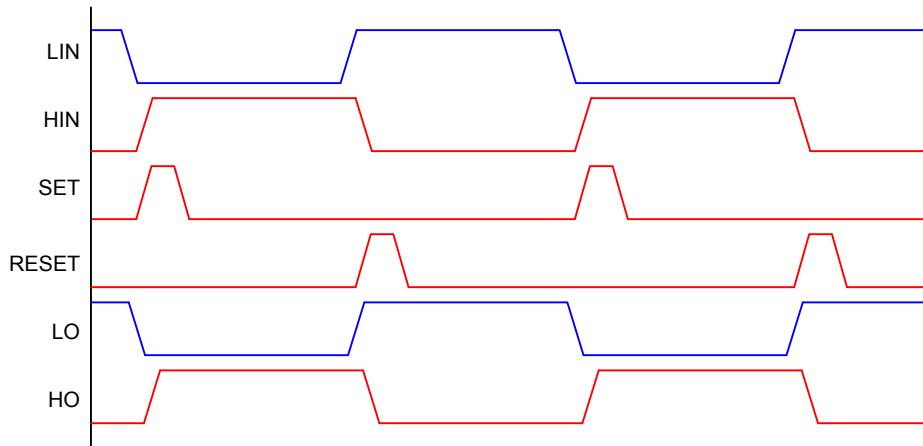


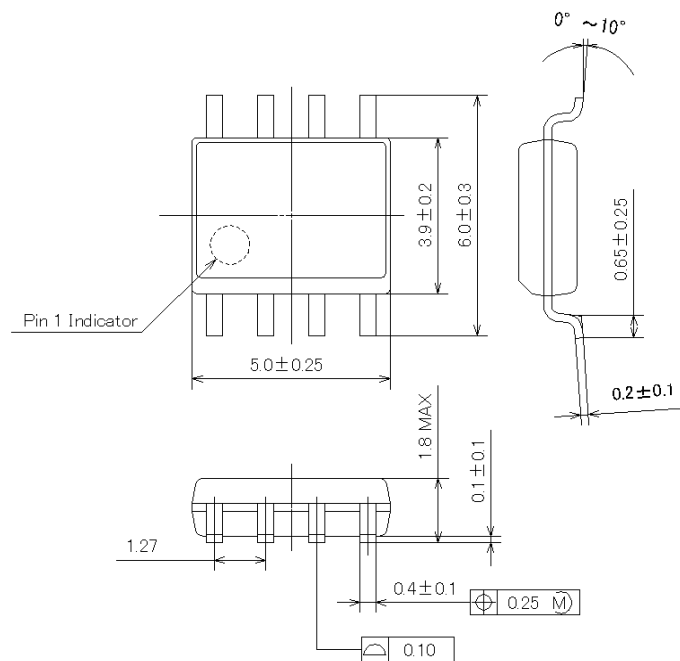
Figure 3. HVIC operation timing chart

HVIC internal blocks are shown in Figure 2. HVIC is composed of input signal detect circuits, level shift circuits, S/N separation circuit, UV detect circuits as well as high side and low side drive circuits.

HVIC operation timing chart is shown in Figure 3. High side input signal HIN is input to the “pulse generator” block and is converted to SET and RESET one-shot pulses based on rise/fall edges. These one-shot pulses are shifted the level by the level shift circuit, and are transmitted to a high side floating circuit. The transmitted signal is shaped by elimination of common mode noise in the “signal/noise separation” block, and is produced by the high side drive circuit as a high side output signal HO. On the other hand, low side input signal LIN is fed to the low side drive circuit through the “timing adjustment” block, and is produced as a low side output signal LO.

5. Outline dimension

FA5650N



Unit: mm

FA5651N

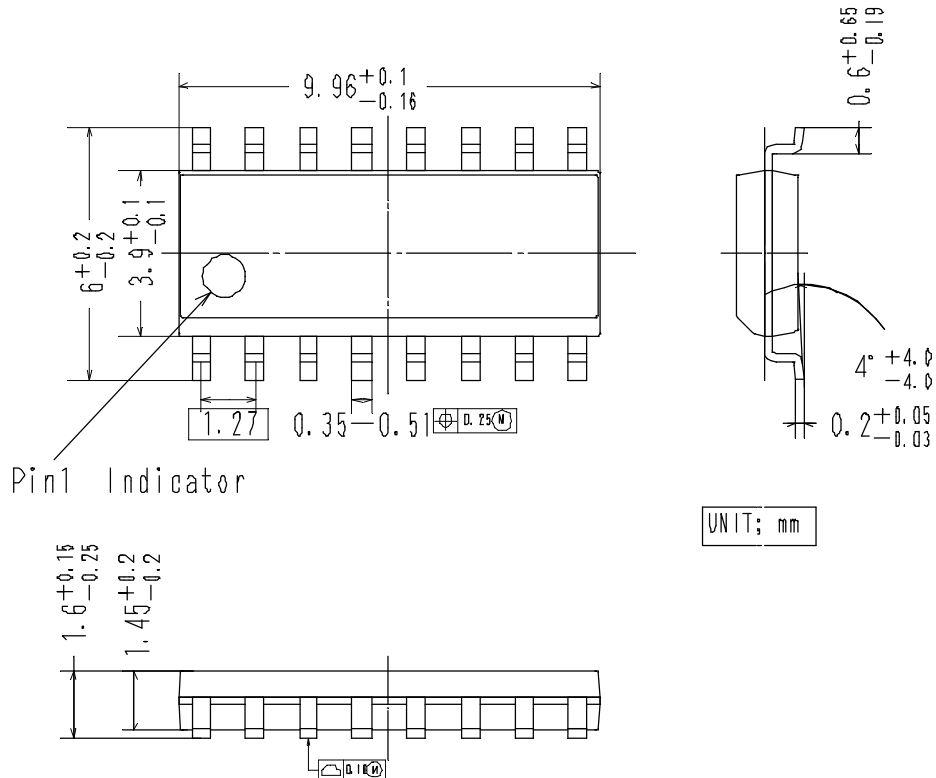


Figure 4. Outline dimension

Note:

High voltage is impressed between pin 5 VCC and pin 6 VS of FA5650N. As the minimum value of the space distance is 0.77 mm, there are cases where sufficient insulation distance cannot be secured depending on the use. In such a case, it is requested to take measures to apply coating of self-extinguishing adhesive, for instance, between terminals.

6. Pin Definitions

FA5650N

Pin	Symbol	Description
1	HIN	Logic input for high-side gate driver output
2	LIN	Logic input for low-side gate driver output
3	GND	Low-side return
4	LO	Low-side gate drive output
5	VCC	Low-side supply (connect capacitor between VCC and GND)
6	VS	High-side floating supply return
7	HO	High-side gate drive output
8	VB	High-side floating supply (connect capacitor between VB and VS)

FA5651N

Pin	Symbol	Description
1	HIN	Logic input for high-side gate driver output
2	LIN	Logic input for low-side gate driver output
3	NC	
4	NC	
5	NC	
6	GND	Low-side return
7	LO	Low-side gate drive output
8	VCC	Low-side supply (connect capacitor between VCC and GND)
9	NC	
10	NC	
11	NC	
12	NC	
13	VS	High-side floating supply return
14	HO	High-side gate drive output
15	VB	High-side floating supply (connect capacitor between VB and VS)
16	NC	

7. Ratings and Characteristics

In defining a current, “+” represents a sink current and “-” a source current.

Absolute Maximum Ratings

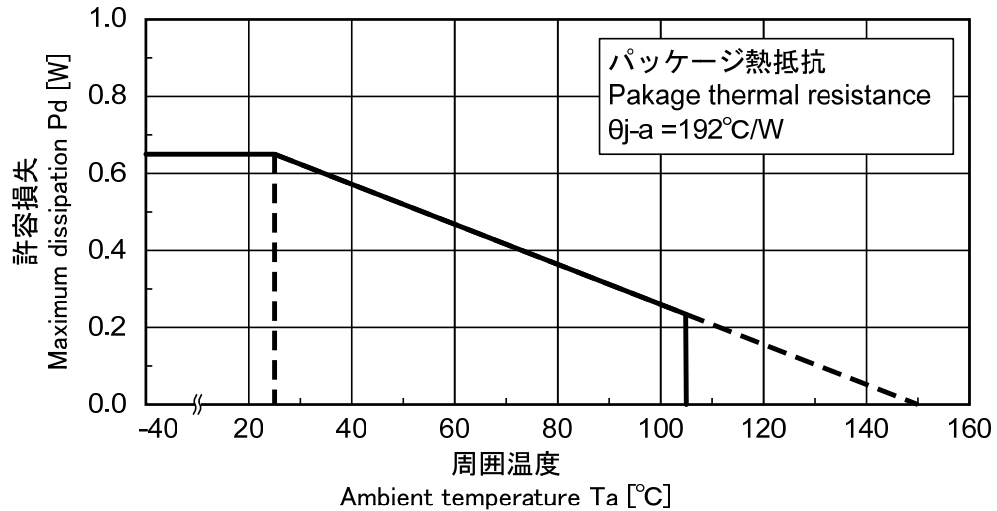
Stress exceeding absolute maximum ratings may malfunction or damage the device.

Never exceed power dissipation Pd.

Item	Symbol	Ratings	Units
High-side floating absolute voltage	VB	-0.3 ~ 830	V
High-side floating absolute current (no switching)	IB	0.05	mA
High-side floating supply offset voltage	VS	VB-30 ~ VB+0.3	V
High-side floating supply offset current (no switching)	IS	0.05	mA
High-side floating supply voltage (VBS=VB-VS)	VBS	-0.3 ~ 30	V
High-side floating supply current (no switching)	IBS	1.5	mA
High-side floating output voltage	VHO	VS -0.3 ~ VB+0.3	V
High-side floating output current (Ta=25°C, VB-VS=30V, PW<1us, 1pulse)	IHO	-1.4 / 1.8	A
Low-side supply voltage	VCC	-0.3 ~ 30	V
Low-side supply current (no switching)	ICC	1.5	mA
Low-side output voltage	VLO	-0.3 ~ VCC+0.3	V
Low-side output current (Ta=25°C, VCC-GND=30V, PW<1us, 1pulse)	ILO	-1.4 / 1.8	A
High-side control input voltage	VHIN	-0.3 ~ 30	V
Low-side control input voltage	VLIN	-0.3 ~ 30	V
Allowable offset supply voltage transient	dVs/dt	±50	kV/us
Maximum input frequency (Within Maximum dissipation)	Fmax	500	kHz
Power dissipation (Ta=25°C)	FA5650N	Pd	650
	FA5651N	Pd	830
Thermal resistance, junction to ambient *1	FA5650N	RthJA	192
	FA5651N	RthJA	120
Operating ambient temperature	FA5650N	Ta	-40 to +105
	FA5651N	Ta	-40 to +125
Operating junction temperature	Tj	-40 to +150	°C
Storage temperature	Tstg	-40 to +150	°C

*1: JEDEC STANDARD Test board

FA5650N



FA5651N

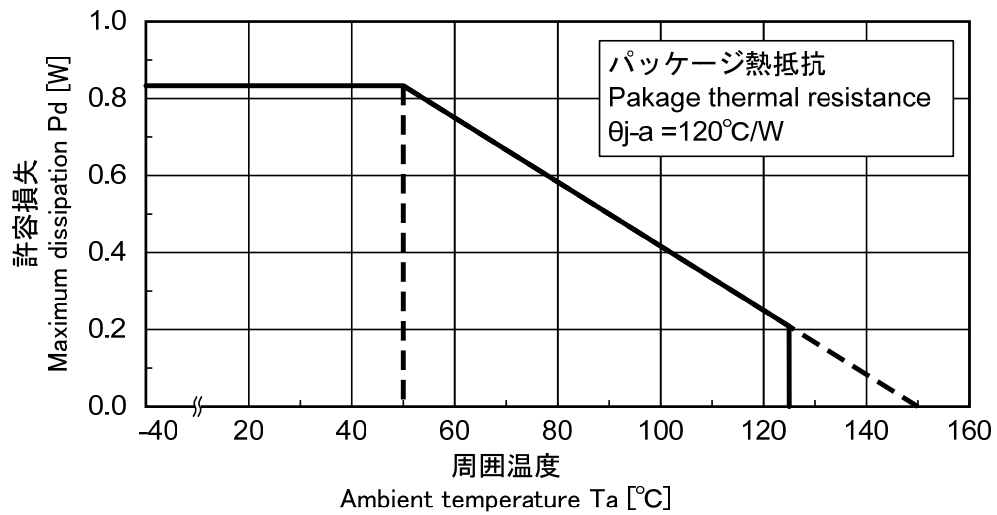


Figure5. Maximum Dissipation Curve

Recommended Operating Conditions

Item	Symbol	Min.	Typ.	Max.	Units	
High-side floating absolute voltage	VB	VS+12	VS+15	VS+18	V	
High-side floating supply offset voltage *2	VS	-5	-	640	V	
High-side floating supply voltage (VBS=VB-VS)	VBS	12	15	18	V	
High-side floating output voltage	VHO	VS	-	VB	V	
Low-side supply voltage	VCC	12	15	18	V	
Low-side output voltage	VLO	0	-	VCC	V	
High-side input voltage	VHIN	0	5	VCC	V	
Low-side input voltage	VLIN	0	5	VCC	V	
High-side input frequency	FHIN	-	-	200	kHz	
Low-side input frequency	FLIN	-	-	200	kHz	
Operating ambient temperature	FA5650N	Ta	-40	-	85	°C
	FA5651N	Ta	-40	-	105	°C

*2: The voltage of the VB pin is over 10V.

DC Electrical Characteristics

T_j=25°C, VCC=15V, VS=GND, VB=15V, HO=open, LO=open, unless otherwise specified.

The voltage described in the condition is DC input and is not AC.

Note) “-” : these items are not guaranteed.

(1) Input (HIN pin, LIN pin)

Item	Symbol	Conditions	Min.	Typ.	Max.	Units
Logic “1” input voltage	V _{IH}	VHIN or VLIN increasing DC input voltage at output voltage high.	1.7	2.1	2.5	V
Logic “0” input voltage	V _{IL}	VHIN or VLIN decreasing DC input voltage at output voltage low.	0.8	1.1	1.5	V
Logic “1” input bias current	V _{IN+}	VHIN or VLIN=5V	10	25	60	uA
Logic “0” input bias current	V _{IN-}	VHIN or VLIN=0V	-	0	5.0	uA
Minimum on pulse width *2	t _{won}	VHIN or VLIN=0V→5V→0V dV/dt=5kV/us	5	40	100	ns
Minimum off pulse width *3	t _{woff}	VHIN or VLIN=5V→0V→5V dV/dt=5kV/us	5	20	100	ns

*2: IC holds off-state if Input on pulse width is smaller than minimum on pulse width.

*3: IC holds on-state if Input off pulse width is smaller than minimum off pulse width.

Relations of input signal and output signal is shown in a figure 6. When pulse width of an input signal is less than minimum on pulse width t_{won} or minimum off pulse width t_{woff}, input signal is not transmitted to the output terminal.

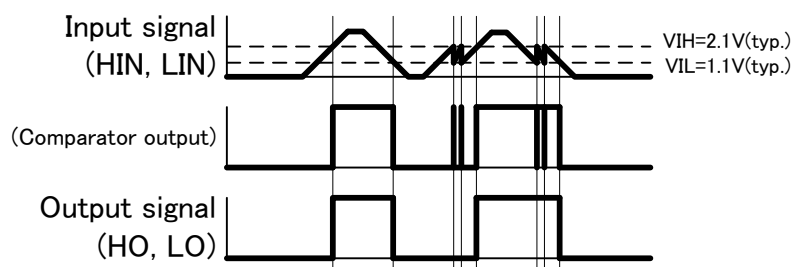


Figure 6. Minimum on/off Pulse Width

(2)Driver Output (HO pin, LO pin)

Item	Symbol	Conditions	Min.	Typ.	Max.	Units
High level output voltage	VOH	VHIN or VLIN=5V Io=-100mA	14.0	14.7	-	V
Low level output voltage	VOL	VHIN or VLIN=0V Io=100mA	-	0.12	0.36	V
Output high short circuit pulse current *4	IOH	Vo=0V, PW<1us, 1pulse	-3.4	-2.3	-1.2	A
Output low short circuit pulse current *4	IOL	Vo=15V, PW<1us, 1pulse	1.4	3.2	5.0	A
Turn-on propagation delay	ton	VHIN or VLIN=0V to 5V dV/dt=5kV/us FHIN or FLIN=100kHz Duty=50%	80	125	170	ns
Turn-off propagation delay	toff	VHIN or VLIN=5V to 0V dV/dt=5kV/us FHIN or FLIN=100kHz Duty=50%	80	125	170	ns
Delay matching, high-side and low-side turn on/off *5	MT	VHIN, VLIN=0V to 5V VHIN, VLIN=5V to 0V dV/dt=5kV/us	-30	0	30	ns
Turn-on rise time	tr	CL=1000pF	3	16	40	ns
Turn-off fall time	tf	CL=1000pF	3	16	40	ns

*4: Guaranteed by design.

*5: MT = ton(HS) – ton(LS), toff(HS) – toff(LS)

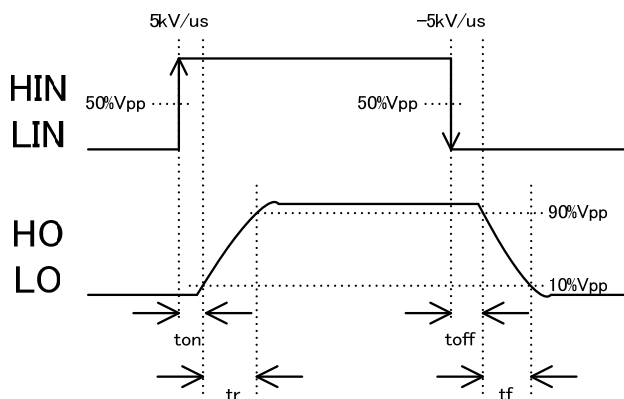


Figure 7. Switching Time Waveform Definitions

(3) Under Voltage Lockout (VCC pin, VB pin)

Item	Symbol	Conditions	Min.	Typ.	Max.	Units
VCC and VBS supply under-voltage positive going threshold voltage *6,7	VBSON VCCON	VBS or VCC Increasing DC Input voltage	8.0	8.9	9.8	V
VCC and VBS supply under-voltage negative going threshold voltage *6	VBSOFF VCCOFF	VBS or VCC decreasing DC Input voltage	7.4	8.2	9.0	V
VCC and VBS supply under-voltage lockout hysteresis voltage	VBSHYS VCCHYS	VBSON-VBSOFF VCCON-VCCOFF	0.3	0.7	1.1	V
VBS supply under-voltage lockout filter time *8	tBSUV	VS=GND, VCC=15V	0.3	1.5	6.0	us
VCC supply under-voltage lockout filter time *8	tCCUV		1	3	10	us
High-side minimum operating voltage *9	VBSMIN	IHO_sink=1mA	1.7	2.9	3.7	V
Low-side minimum operating voltage *9	VCCMIN	ILO_sink=1mA	1.7	2.9	3.7	V

*6: Positive going threshold voltage > Negative going threshold voltage

*7: In the case of $2.5V/\mu s < dV_{CC}/dt < 10V/\mu s$, the LO pin has a possibility of outputs on-pulse.

*8: • VBS(VCC) supply under-voltage lockout filter time: tBSUV increasing (tCCUV)

It is the time to VHO(VLO)=H, after VBS(VCC) voltage reaches the VBS(VCC) supply under-voltage positive going threshold voltage.

• VBS supply under-voltage lockout filter time: tBSUV decreasing

It is the time to VHO=L, after VBS voltage reaches the VBS supply under-voltage negative going threshold voltage.

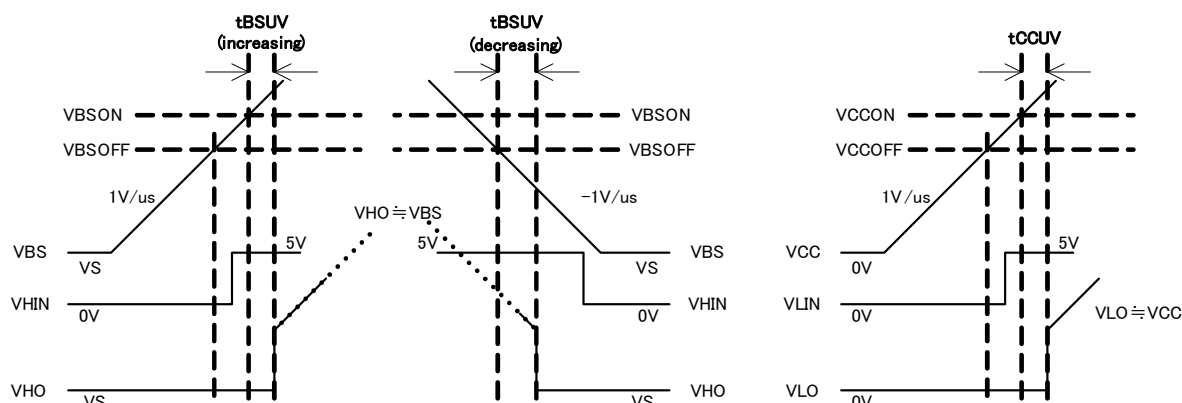


Figure 8. UVLO filter time Definitions

*9: In the case of $(V_B - V_S) < V_{BSMIN}$ or $V_{CC} < V_{CCMIN}$, the switching device may operate abnormally because the HO pin output or the LO pin output turns on regardless of the HIN input or the LIN input. Reference to “10. Design Guidelines”.

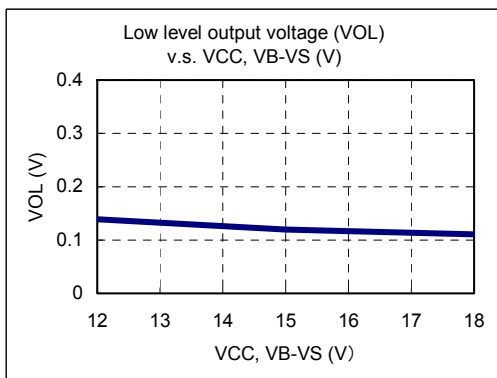
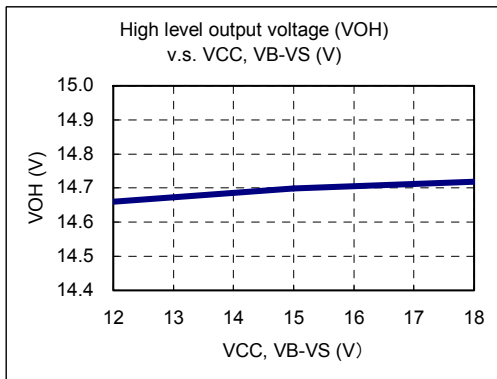
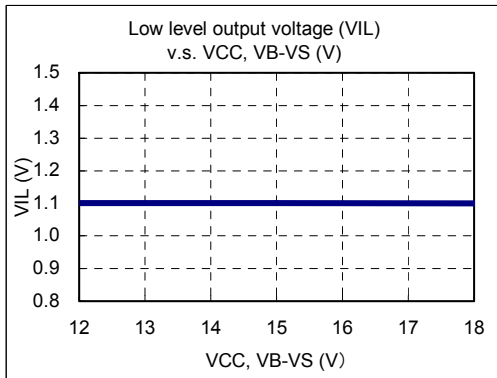
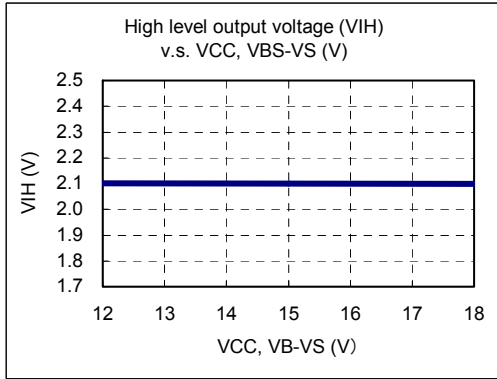
(4) Power Supply Current (VCC pin, VB pin)

Item	Symbol	Conditions	Min.	Typ.	Max.	Units
Offset supply leakage current	ILK	VB=VS=800V VHIN=VLIN=0V	-	0	1	uA
Quiescent VBS power supply current	IBS	VHIN=VLIN=0V DC Input voltage	20	60	150	uA
Quiescent VCC power supply current	ICC	VHIN=VLIN=0V DC Input voltage	280	400	520	uA
Dynamic operating power supply current	IOP	VHIN=VLIN=0V↔5V FHIN=FLIN=100kHz Duty=50% dV/dt=5kV/us	0.5	1.0	2.0	mA

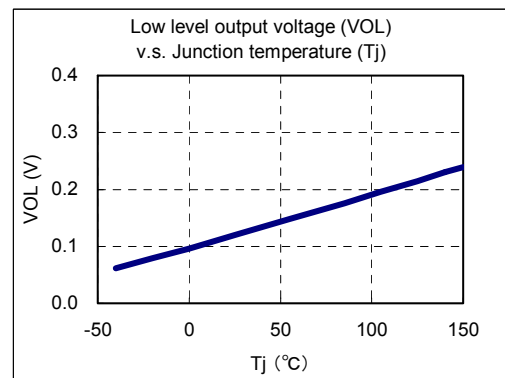
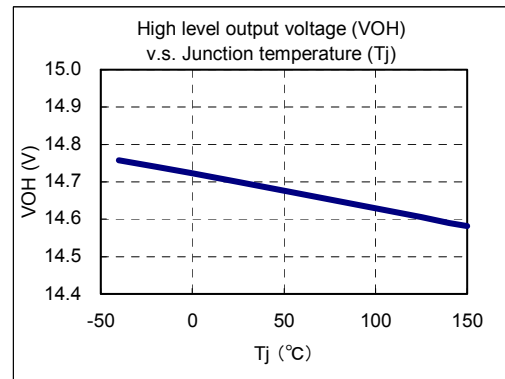
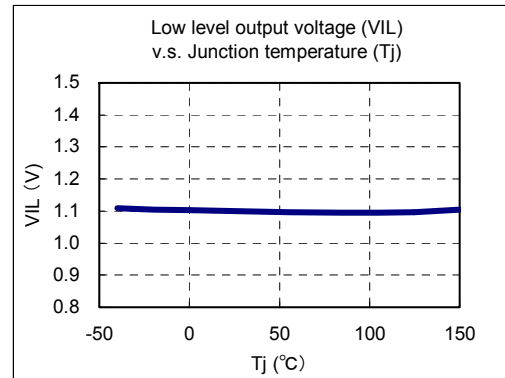
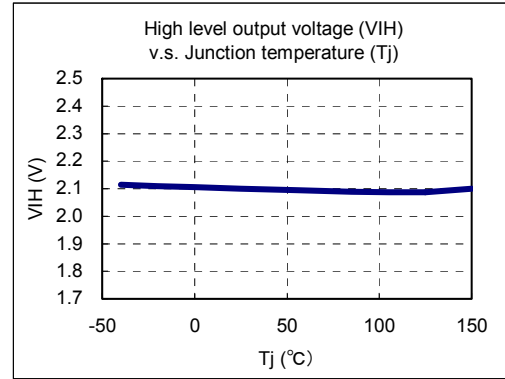
8. DC Typical Characteristics

$T_j=25^\circ\text{C}$, $V_{CC}=15\text{V}$, $V_S=\text{GND}$, $V_B=15\text{V}$, $H_O=\text{open}$, $L_O=\text{open}$, unless otherwise specified.

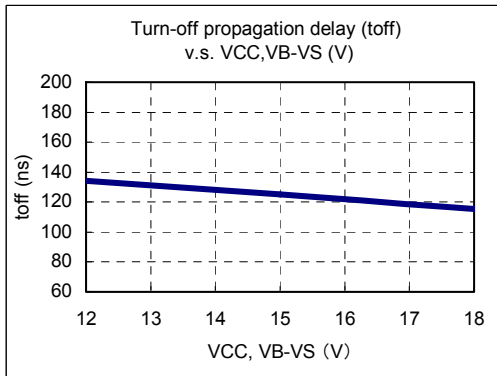
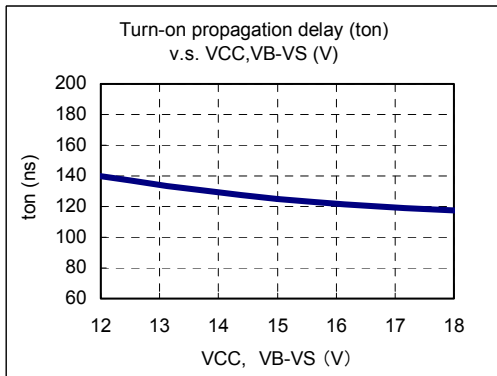
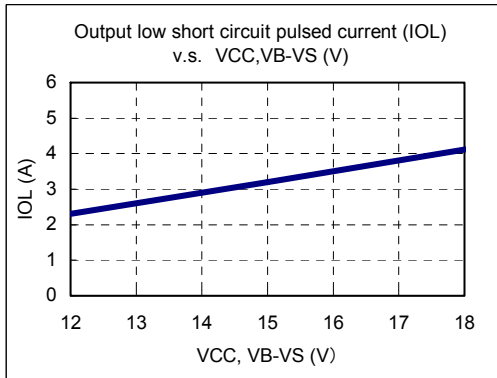
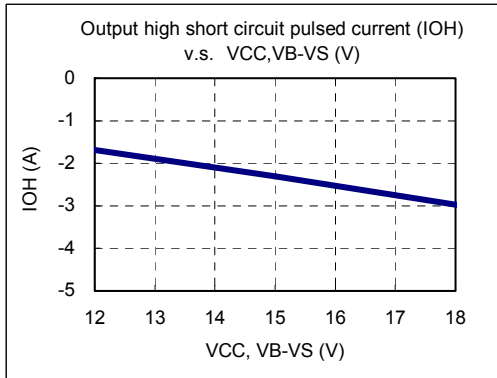
Voltage-dependence



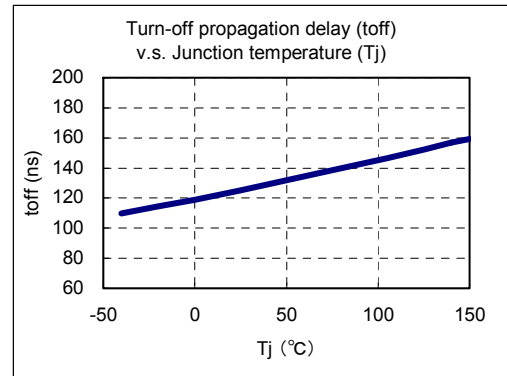
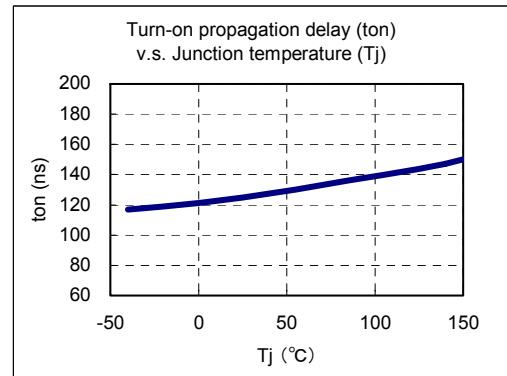
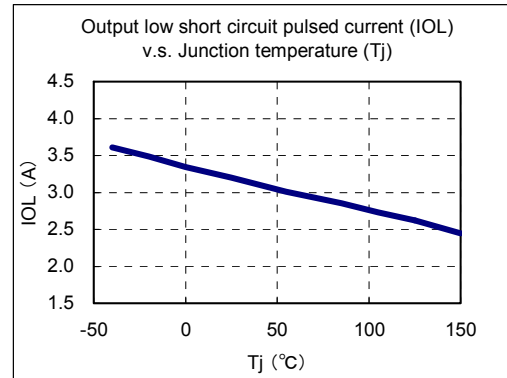
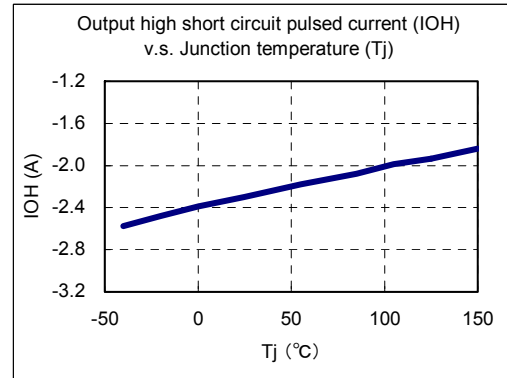
Temperature-dependence



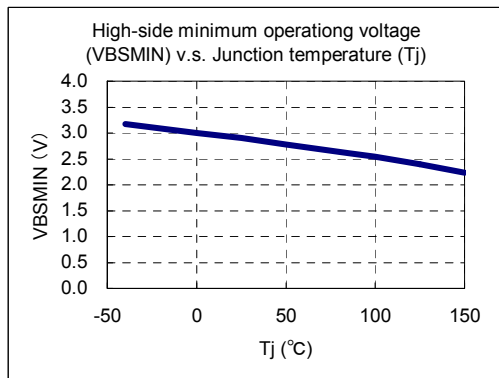
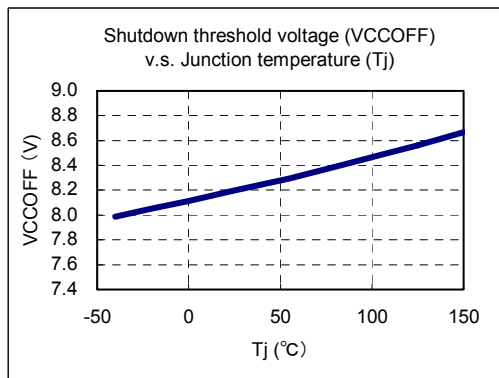
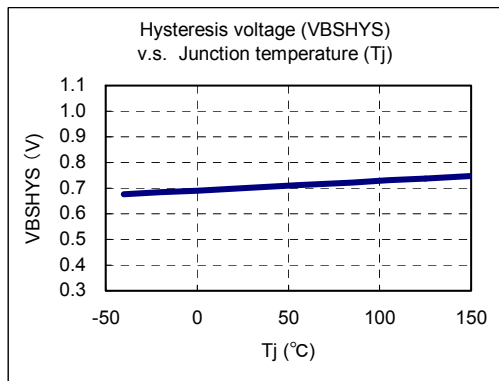
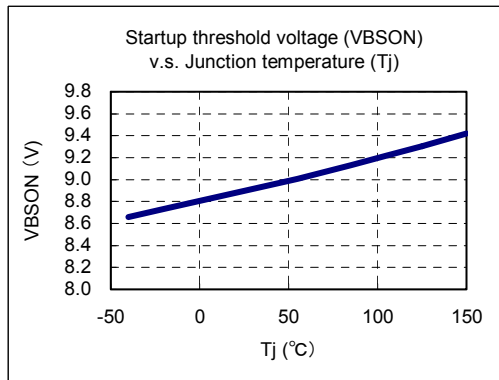
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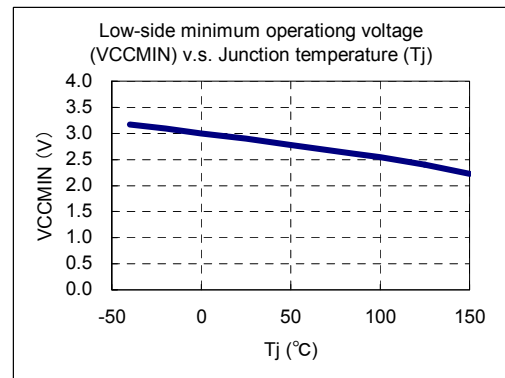
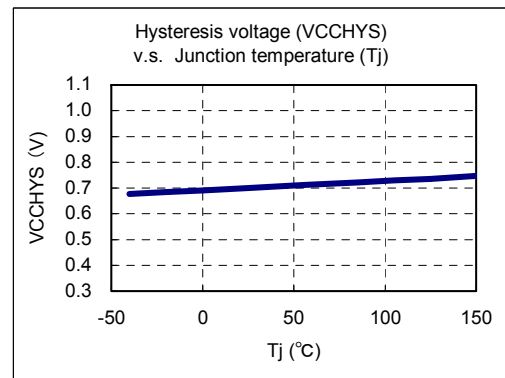
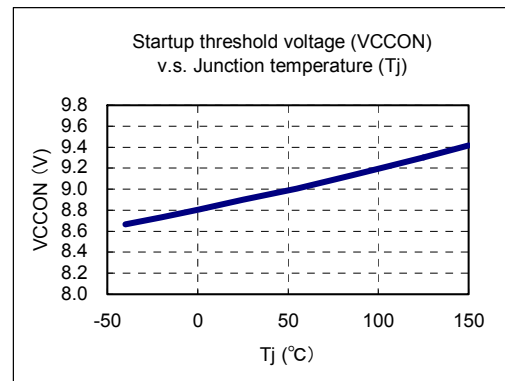
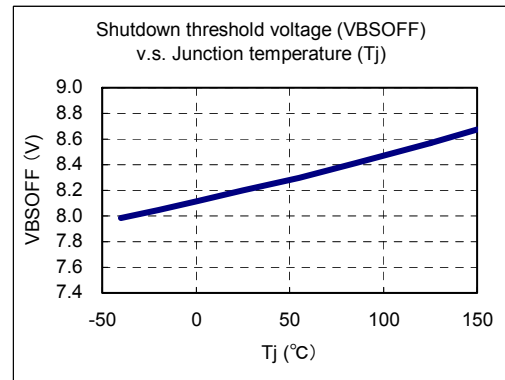
Temperature-dependence



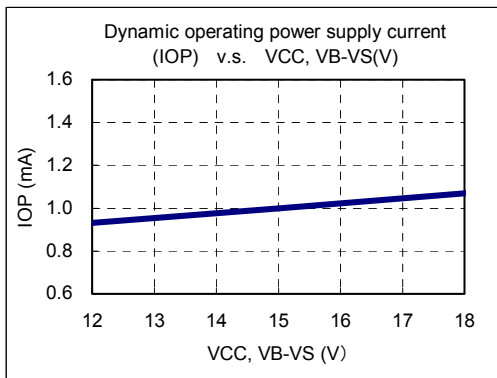
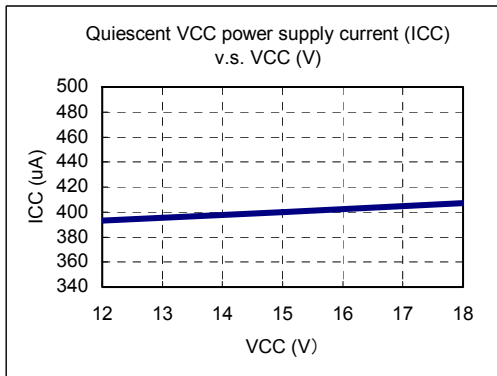
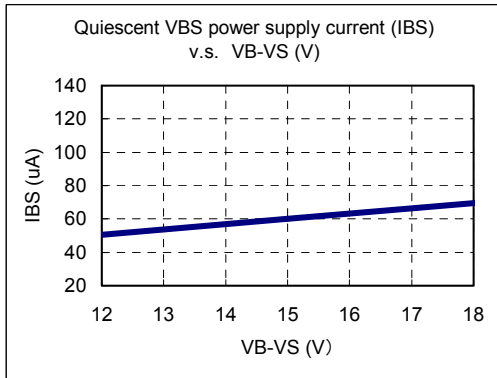
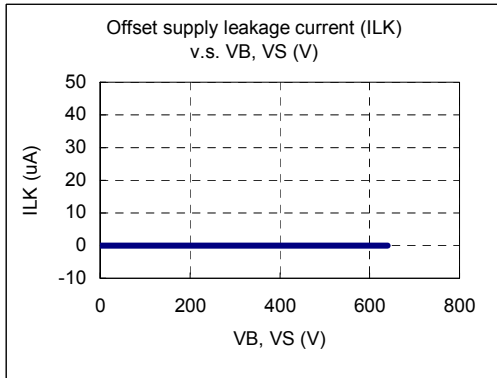
Temperature -dependence



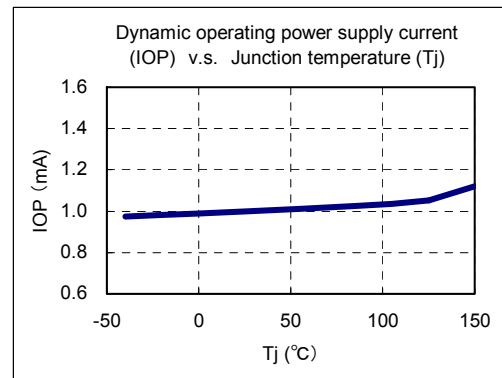
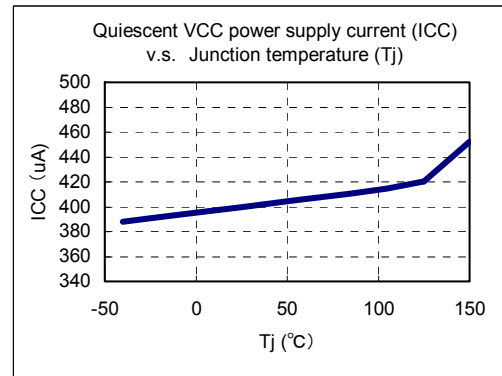
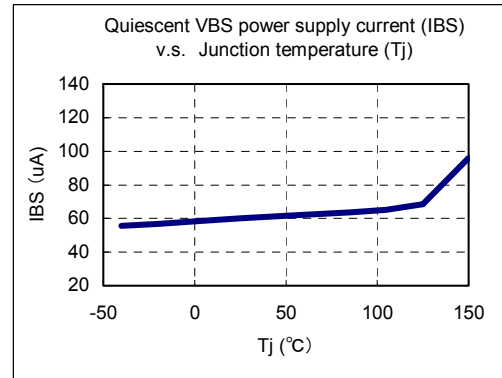
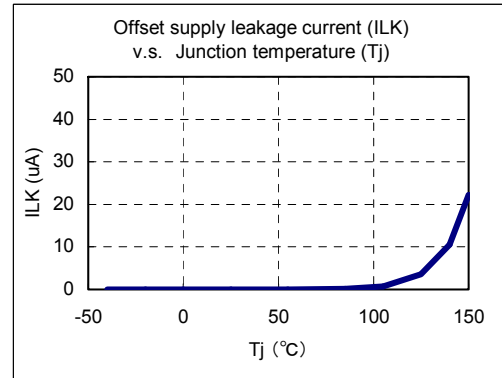
Temperature-dependence



Voltage-dependence



Temperature-dependence



9. Start/stop operation

Low side operation is shown in Figure 9. At the time of power supply rise, the LO output is indeterminate while the voltage is minimum operating voltage VCC_{MIN} or less. The LO output is produced when the voltage rises to ON threshold voltage VCC_{CON} or greater.

At the time of power supply fall, the LO output stops when the voltage drops to OFF threshold voltage VCC_{OFF} or less. When the voltage further drops to VCC_{MIN} or less, the LO output becomes indeterminate. The LO operation is not dependent on high side power supply voltage VBS.

The high side operation is shown next. Figure 10 shows the case where VCC rises and falls from the state where VBS is established. When the voltage rises to ON threshold voltage VCC_{CON} and HIN is input, the HO output is produced. When the voltage drops to OFF threshold voltage VCC_{OFF} or less, the HO output stops. In this case, there is no state where the HO logic becomes indeterminate.

Figure 11 shows the case of rise/fall of VBS from the state where VCC is established. When the voltage rises to ON threshold voltage VB_{SON} or greater and HIN is input, the HO output is produced. When the voltage drops to OFF threshold voltage VB_{SOFF} or less, the HO output stops. At VB_{SMIN} and less, the HO output is indeterminate.

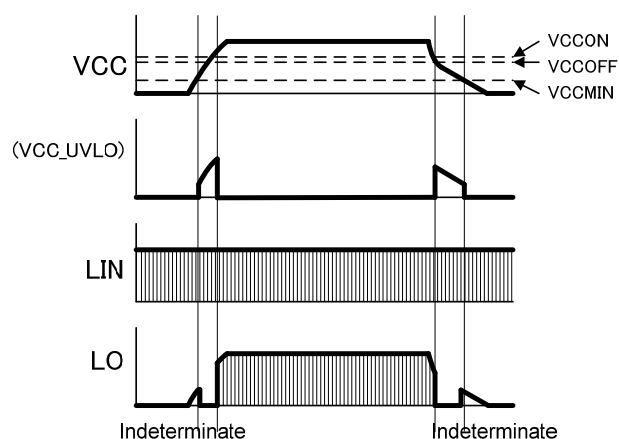


Figure 9. Low side operation of VCC rising/falling

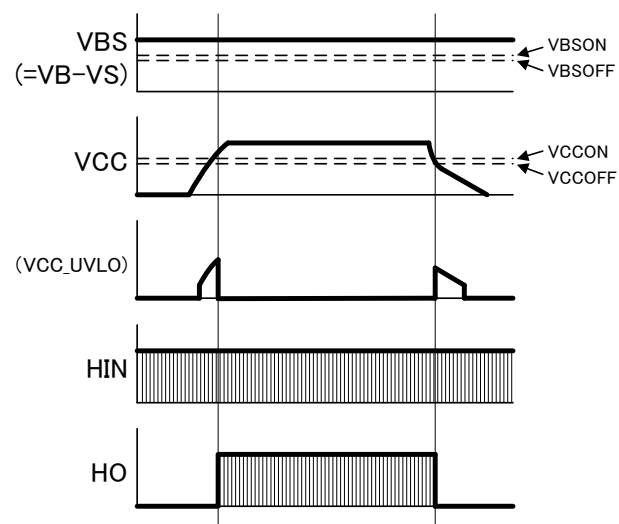


Figure 10. High side operation of VCC rising/falling when VBS is established

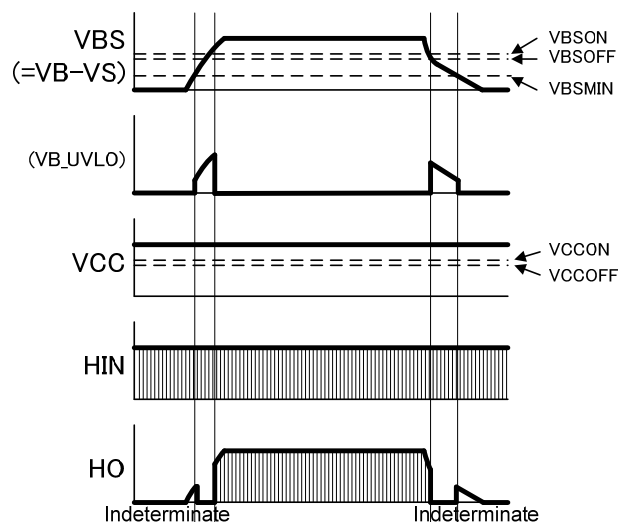


Figure 11. High side operation of VBS rising/falling when VCC is established

10. Design Guidelines

10.1 Prevention of high-side MOSFET self-turn-ON

In the case where VBS or VCC is lower than the minimum operating voltage, the output signal (HO, LO) may appear without regard to the input signal (HIN, LIN). Especially in the case where VBS is lower than the minimum operating voltage VBSMIN, since the HO voltage is undefined, turning on of the low-side MOSFET might cause a self turning on of the high-side MOSFET by the ratio between the reverse transfer capacitance Crss and the input capacitance Ciss of the high-side MOSFET. In such a case, set an appropriate capacitor Cadd between the gate and the source of the high-side MOSFET for avoiding the rise of the gate voltage, or do not use a MOSFET of low threshold voltage VGS (th). Select the appropriate capacitance Cadd referring to the following formula. As a high voltage power MOSFET has a characteristic of rapid decreasing Crss after Vds exceeds around 10V and the influence of Crss for the gate voltage becomes smaller, put the amount of Vds changing as ΔVds from 0V to the value near the selected Crss. And as VGS (th) has a characteristic becoming lower at the higher temperature, select the capacitance Cadd having enough margin by considering a higher temperature condition.

$$VGS(th) > \frac{Crss}{Ciss - Crss + Cadd} \times \Delta Vds$$

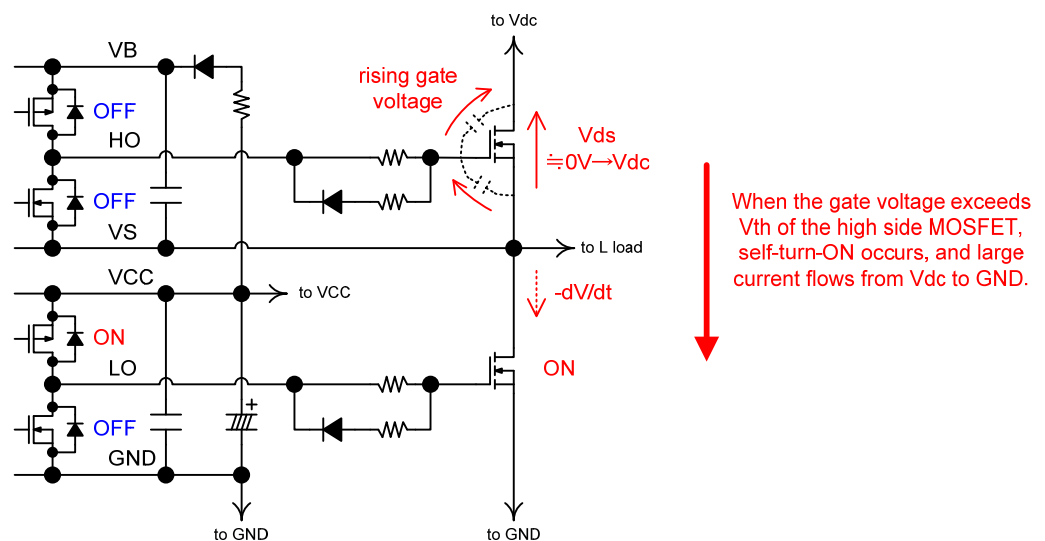


Figure 12. Lifting of high-side FET's gate voltage when the low-side FET turns on

10.2 Application circuit which use FWD positively

In applications such as motor control we have positive switching operations of a built-in diode of MOSFET, or of a freewheel diode FWD which is a reverse parallel connection to IGBT. In the case of IGBT, when the high side IGBT turns on while current is flowing through FWD of the low side IGBT, reverse-recovery-current into the FWD will make a steep dV/dt . And the rapidly rising of the voltage between the collector and the emitter by this steep dV/dt will raise the gate voltage by the current flowing through the capacitance between the gate and the collector. As the result, you will see the problem of increasing the turn-on loss of IGBT. Take the following measures to avoid this problem.

- Reduce dV/dt by slowing the turning-on speed.
- Reduce the impedance between gate and emitter by reducing the turning-off resistance.
- Reduce the wiring impedance by minimizing the wiring distance between HVIC and IGBT.
- Add a gate-reverse-biasing circuit.

Since this HVIC has no built-in reverse-biasing circuits, it is necessary to mount buffer circuits with a built-in reverse-biasing circuit between the HVIC and the power devices, in the case that power devices are used in reverse-biased at turning-off.

10.3 Impressing of negative voltage to high-side VS pin

When Q1 of the high-side MOSFET is turned off from on-state while Q2 of the low-side MOSFET is off, the current which was flowing through Q1 circulates through the body diode of Q2 and the load. At this moment, by the inductance and the current changing rate, the VS terminal voltage falls tens of volts from the ground potential voltage during the period of hundreds of ns, and so IC may malfunction or break when absolute maximum rating is exceeded.

Fuji HVIC secures high negative-withstand-voltage by contriving the device layout in IC. (Negative-withstand-voltage means the voltage in which output signals do not malfunction to input signals.) The following figure shows the typical measurements of the negative-withstand-voltage against the pulse width. Fuji HVIC has negative-withstand-voltage of 3 or more times than competitor's at the time of pulse width 1us, and has the feature which may not malfunction easily. As the result, Fuji HVIC has advantage when the design does not permit the reduction of the switching speed or of the parasitic inductance of wiring patterns.

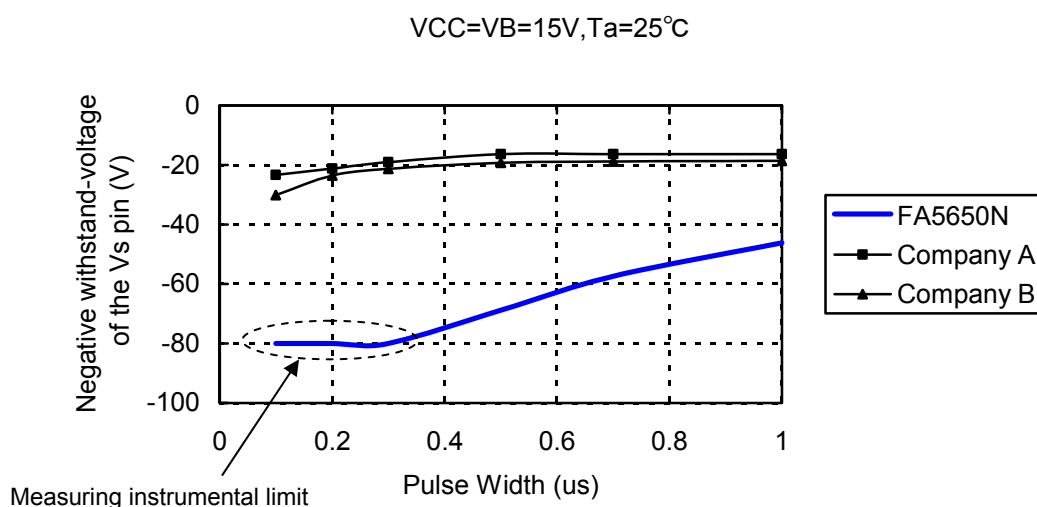


Figure 13. Comparison of negative-withstand-voltage tolerance of VS pin
(The data described here indicates typical IC characteristics, and does not guarantee characteristics.)

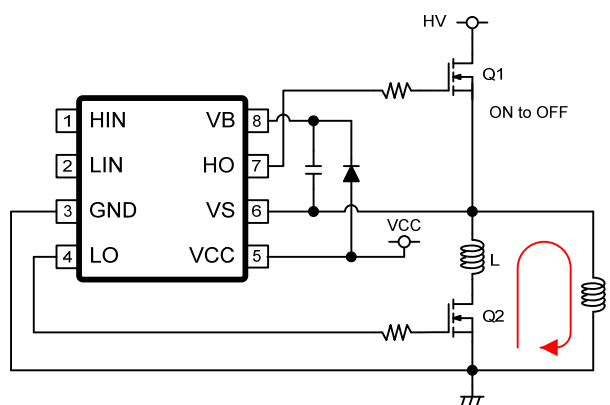


Figure 14. Impressing negative voltage to VS pin

10.4 Bootstrap Circuit for High-side gate drive power supply

Driving the high side MOSFET Q1 requires the power supply voltage VBS based on the Q1's source potential voltage. The high side power supply voltage VBS easily consists of an external bootstrap circuit. And it has an advantage that the system cost can be lower than preparing floating power supplies for VBS.

(1) Basic Operation of Bootstrap Circuit

When the low side MOSFET Q2 turns on, VS voltage is reduced to the ground potential and the low side power supply VCC charges the capacitor C1 through the diode D1. When Q2 turns off, VS becomes a floating potential and the charging loop is shut off. And the electric charge of C1 will drive Q1, being HIN inputted.

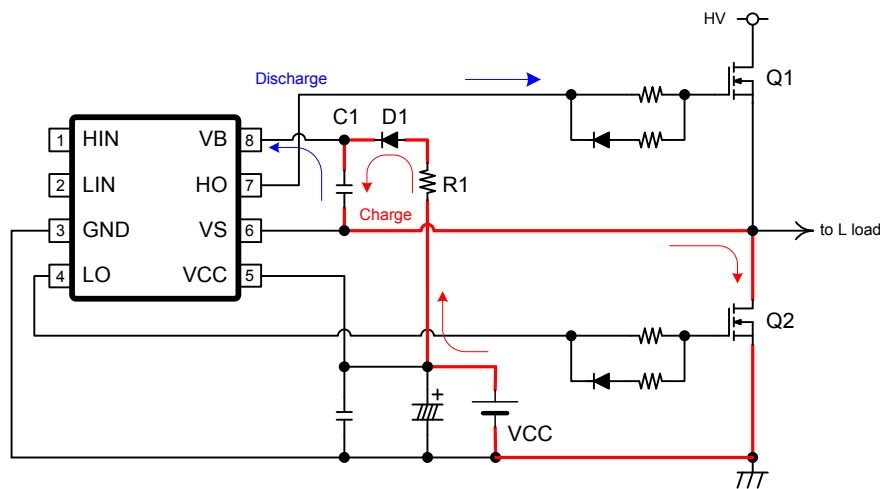


Figure 15. Basic Operation of Bootstrap Circuit

(2) Selection the Bootstrap Capacitor C1

When Q2 is off-state and Q1 is being driven, the high side power supply voltage VBS is reduced gradually through the high side operating current IBS, the gate charging current of Q1 and the leakage current of C1 since C1 is not being charged. Therefore, it is necessary to select the capacitance of C1 so that VBS voltage may not fall to below the off-threshold-voltage VBSOFF while Q1 is being driven. The capacitance indispensable for C1 is calculated by the following formula. We recommend that the C1 value is twice or more than the calculated.

$$C1 = \frac{Qg + IBS \times Ton + Icb(Leak) \times Ton}{Vcc - VBSOFF - Vf - VLS}$$

Qg: Gate charging amount of MOSFET, IGBT (Q1)

IBS: High side operating current of IC

Ton: High side maximum on time

Icbs (leak): Leak current of bootstrap capacitor (C1)

VCC: Low side power supply voltage

VBSOFF: High side off threshold voltage

Vf: Diode forward direction voltage of bootstrap (D1)

VLS: On voltage of low side MOSFET, IGBT (Q2)

We can charge the capacitance C1 only while the low side MOSFET Q2 is on-state (and the high side MOSFET Q1 is on). And it is necessary to set the on-state period Ton2 of Q2 so that the q electrically discharged from C1 while Q2 is off can be fully recharged.

$$q = CE(1 - e^{-\frac{ton2}{CR}})$$

C: Capacitance of C1

E: Voltage impressed between the both ends of C1

CR: Time constant of the series circuit C1 and R1

(3) Selecting the Bootstrap Diode D1

Select the fast recovery diode with a short reverse recovery time. Using a diode for D1 with a long reverse recovery time decreases the power supply efficiency of VCC (the low side power supply) since the reverse recovery current to VCC becomes large when high-side is on. And ripples to VCC might cause malfunction. Select the diode having a withstand voltage more than the low-side power device, considering of derating. For instance, to use Fuji's FMV11N60E for the low-side power device, it is necessary to select the diode for D1 having a withstand voltage exceeding 600V.

The average current IFAV can be roughly calculated by the product of the total gate-charging amount Qg and the operating frequency fsw of the power device. When Qg=73nC(max) and fsw=100kHz are assumed, IFAV can be calculated by the following.

$$IFAV = Qg \times fsw = 7.3mA$$

And the peak current can be calculated by dividing the maximum low side power supply voltage VCC by the resistance R1.

(4) Selecting of Resistor in Series with Bootstrap Diode

Make sure to insert the resistor R1 preventing the initial rush current charging C1. And to prevent breaking the diode D1, select the resistance of R1 so that the current flowing into D1 is absolutely below the peak current acceptable of D1.

(5) Other Guidelines

- The high side power supply voltage VBS is lower than the low side power supply voltage VCC due to the on-state voltage of D1 and Q2, and, in addition, due to the on-state period of Q2. Thus, it is necessary to take notice of the difference of the gate voltages of Q1 and Q2.
- If Q1 switches and Q2 keeps off-state, the VBS voltage falls rapidly and the HO terminal might be easily suspended.
- At the startup, it is necessary to charge C1 initially by turning on Q2. And secure the on-period of Q2 so that the voltage of C1 should be set high enough to the off-threshold voltage VBSSOFF.
- As is described above, there are constraints in preparing high side power supplies by bootstrap circuits. If some problems arise from using bootstrap circuits, we recommend using DC/DC converters insulated by the transformer to make stable power supplies to HVIC.
- When using IGBT as power devices, not using power MOSFET, the saturation voltage Vce (sat) between the collector and the emitter very depends upon the gate voltage. Lower gate voltage makes the saturation voltage higher, and increases the steady-state loss. Thus, set the power supply voltage to be able to secure the recommended gate voltage described in the IGBT data sheet. In general, the recommended IGBT's gate voltage is 15V, and the power MOSFET's is 10V.

10.5 Layout Guidelines

Consider the points described below in the pattern layouts. Design the patterns to satisfy the safety standards in the countries or the areas where the products are used. And check the layout patterns and the circuit constants fully enough in the actual products.

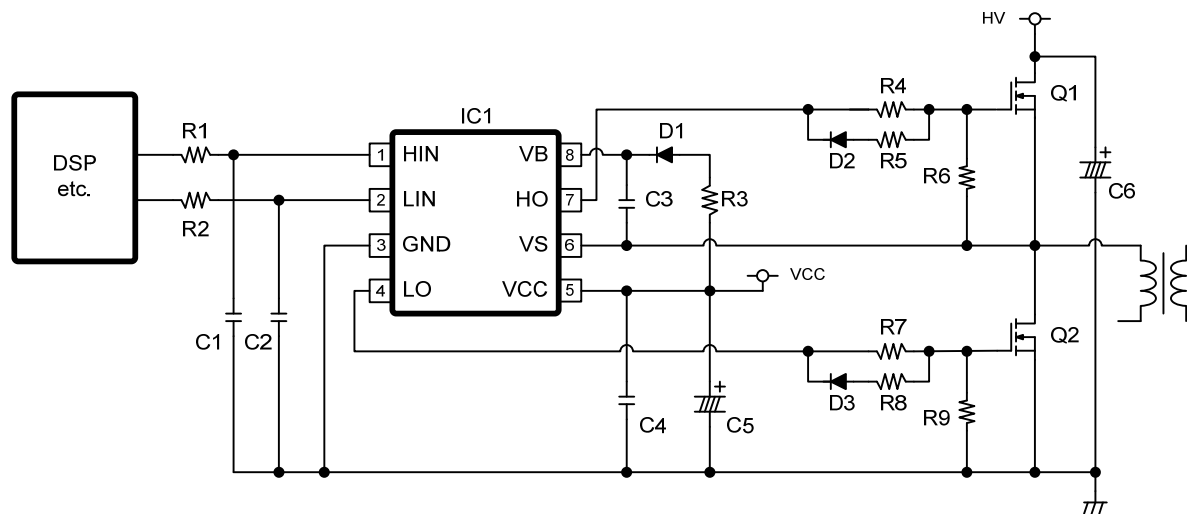


Figure 16. Typical circuit

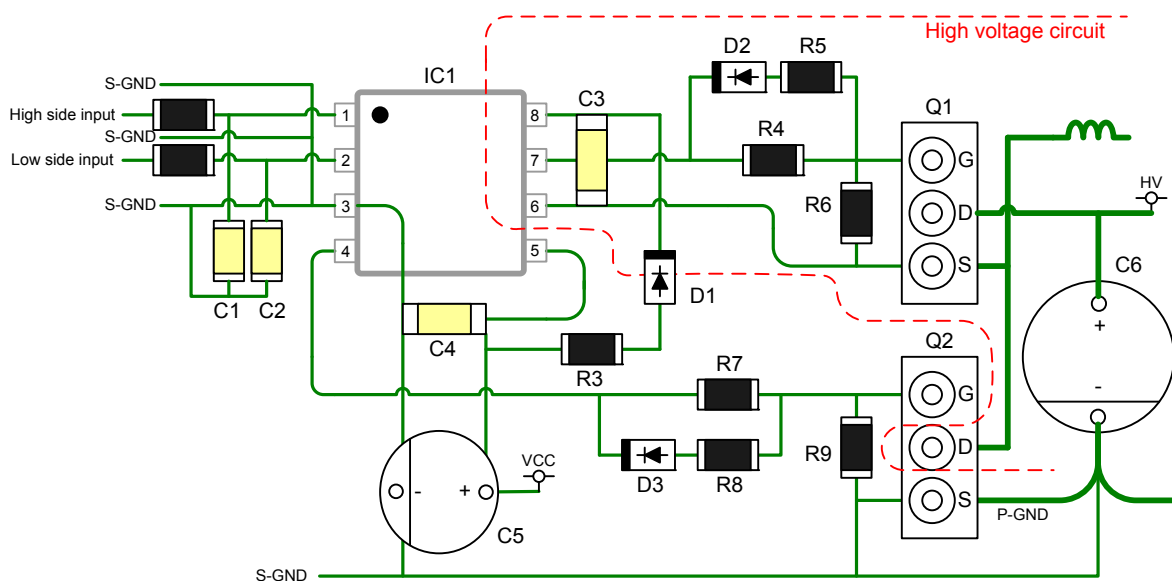


Figure 17. Typical layout

- Separate the power line P-GND in which the main current flows from the signal line S-GND in which the control current flows. If both are in common, S-GND's electric potential is fluctuated by the main current and the product may malfunction.
- If noises influence the input signals of IC, CR filters must be arranged near by the pin No.2 (HIN) and the pin No.3 (LIN).
- It is recommended to arrange the S-GND patterns adjacent to the HIN line and the LIN line, in order to avoid cross talks between HIN and LIN and to reduce interference between parallel lines on the printed circuit board.
- Arrange the HIN, LIN and S-GND patterns away from the power circuits.
- Not to receive the induction noise, minimize the loop area made by the power supply pattern driving a gate and by the gate terminal. Larger loop area might cause over-voltage destruction or malfunction of the MOSFET. And do keep the P-GND pattern from passing to this gate current loop.

- Arrange the bootstrap capacitor C3 near by the pin No.6 (VS) and the pin No.8 (VB).
- Minimize the loop area made by Q1, Q2 and C6 patterns. It is effective for suppressing the surge voltage and the radiation noise of the power devices.
- The surge voltage generated between VS and GND can be suppressed by reducing the pattern inductance of VS, Q1 source, Q2 drain, Q2 source and GND pin.

11. Truth Table

Input				Output	
HIN	LIN	VCC	VBS	HO	LO
-	-	L	L	L	L
-	-	L	H	L	L
-	L	H	L	L	L
-	H	H	L	L	H
L	L	H	H	L	L
H	L	H	H	H	L
L	H	H	H	L	H
H	H	H	H	H	H

When VCC or VBS increases:

“L” means the state below the ON threshold voltage.

“H” means the state above the ON threshold voltage.

When VCC or VBS decreases:

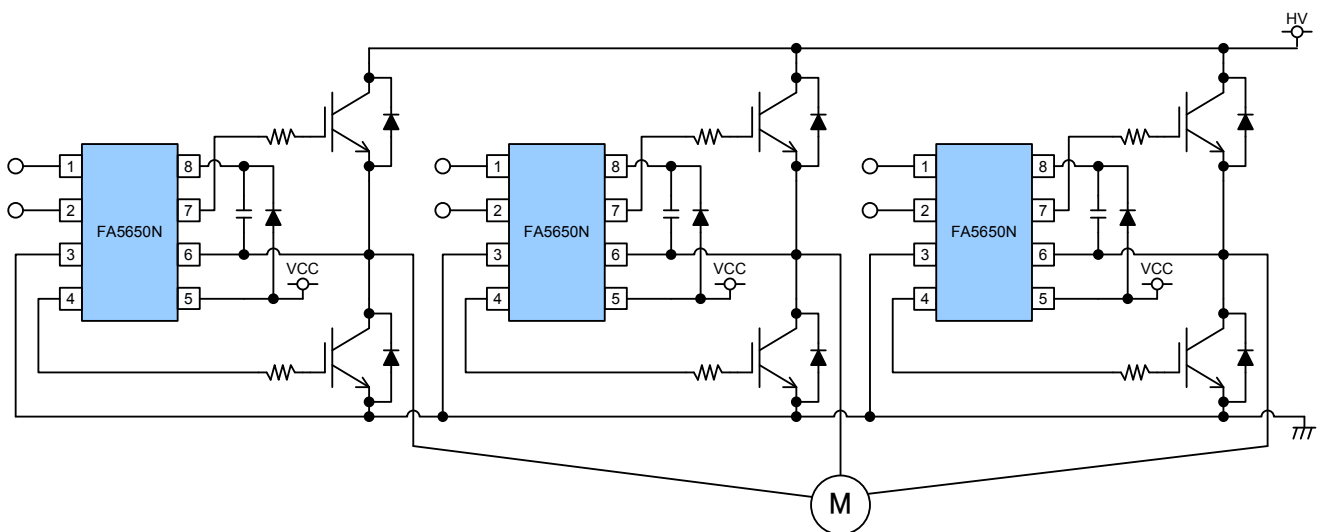
“L” means the state below the OFF threshold voltage.

“H” means the state above the OFF threshold voltage.

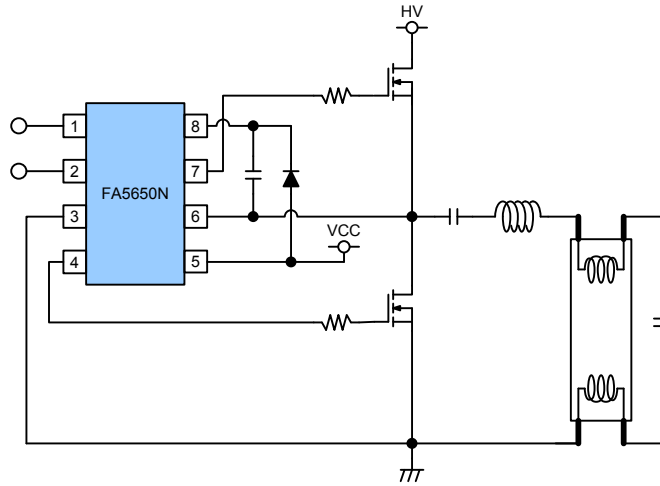
12. Typical applied circuit

Typical HVIC application circuits are shown below.

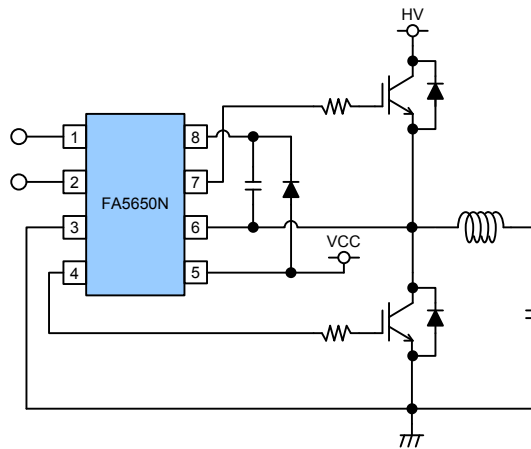
(1) Motor drive (general-purpose inverter, AC servo, air-conditioner, clothes washing machine)



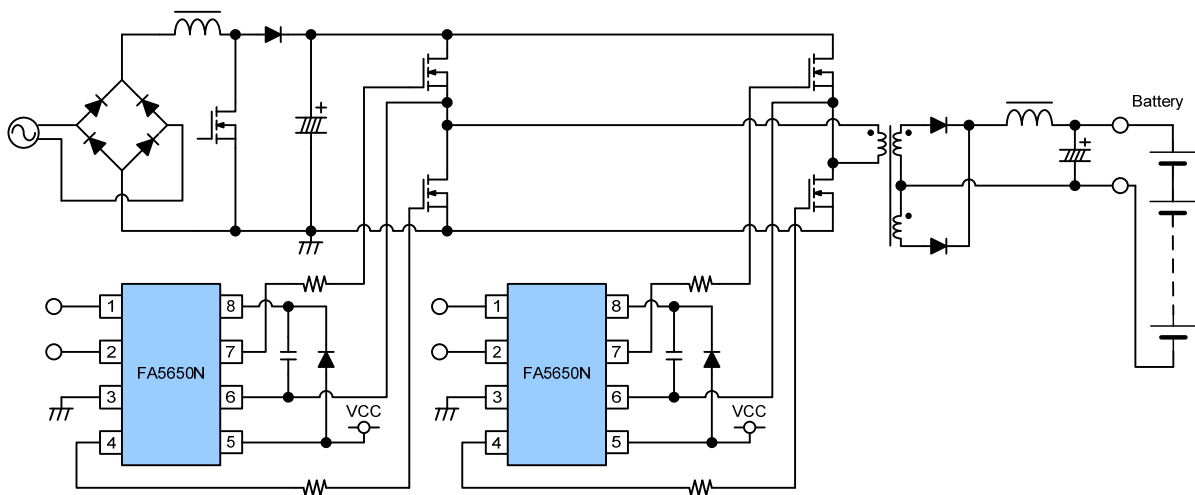
(2) Inverter fluorescent lamp



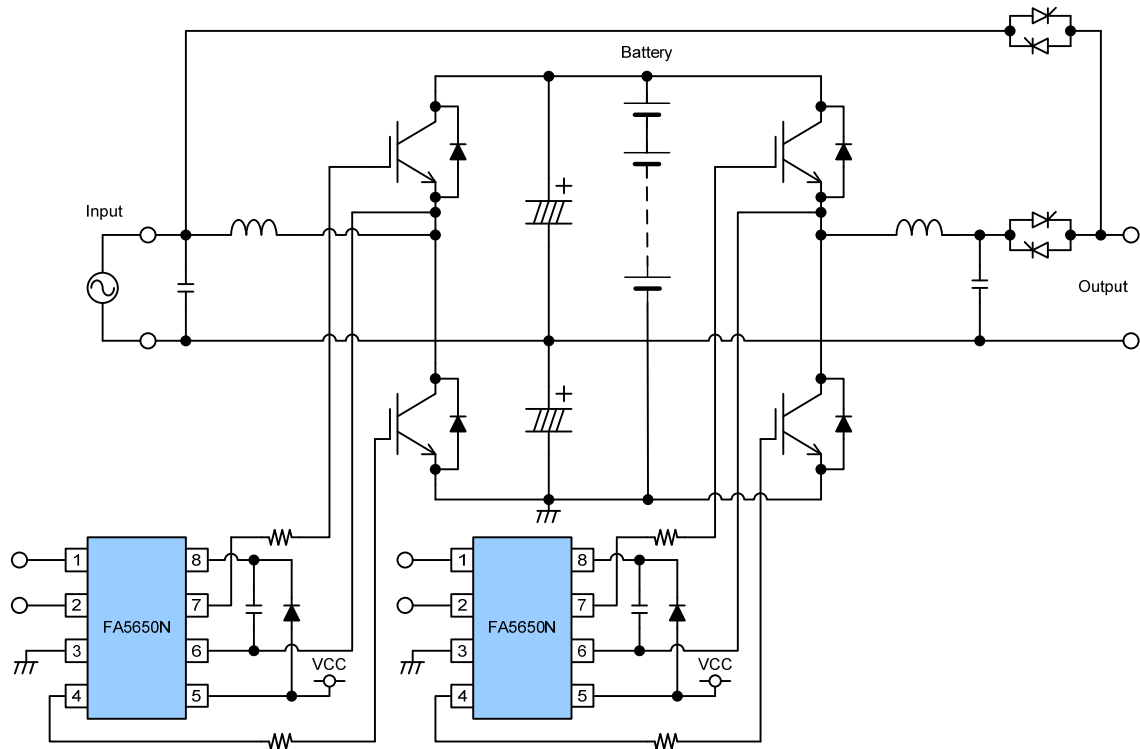
(3) IH cooking heater



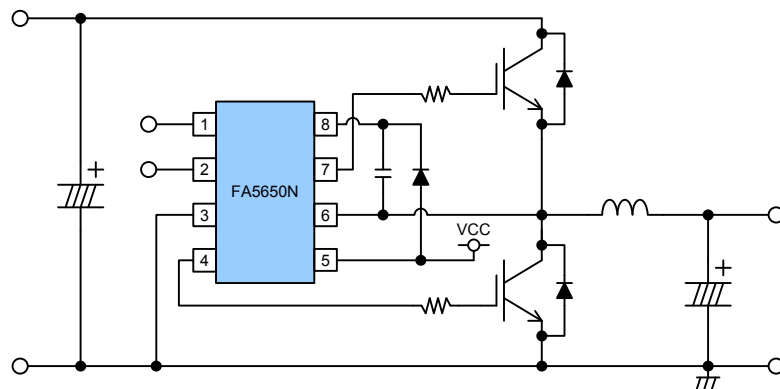
(4) AC/DC converter (battery charger)



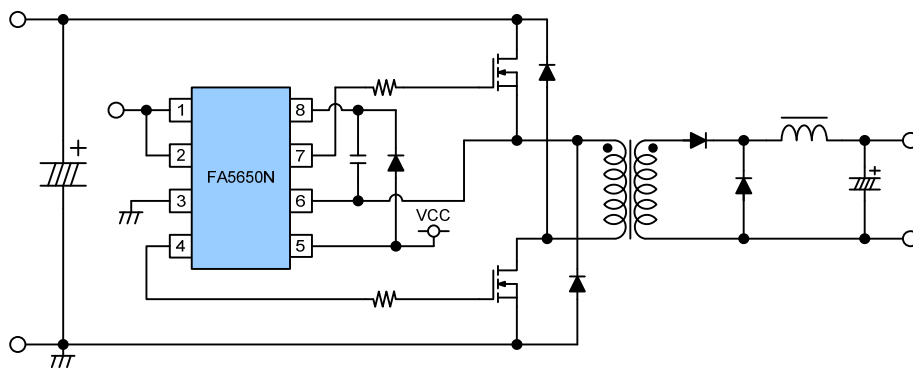
(5) UPS



(6) Buck/Boost chopper



(7) Double forward Converter



Be aware that a high-side power supply voltage made by a bootstrap circuit drops since VS voltage does not fall to GND voltage, in the case of a double forward converter circuit.

13. Compared with an Optocoupler method

In order to drive the power devices of a high-side by the control signals of a low-side, both must be insulated electrically. As the one method, an optocoupler method to insulate optically is generally used. We compare a HVIC method with a optocoupler method below.

The list below shows the difference between a HVIC method and a optocoupler method. A HVIC method has an overwhelming advantage of short signal transfer time. Therefore, HVIC suits for high-frequency switching and for fast response. And Fuji HVIC has improved the allowable negative voltage on the floating terminal VS which might cause malfunction, so it can be applied to larger power applications.

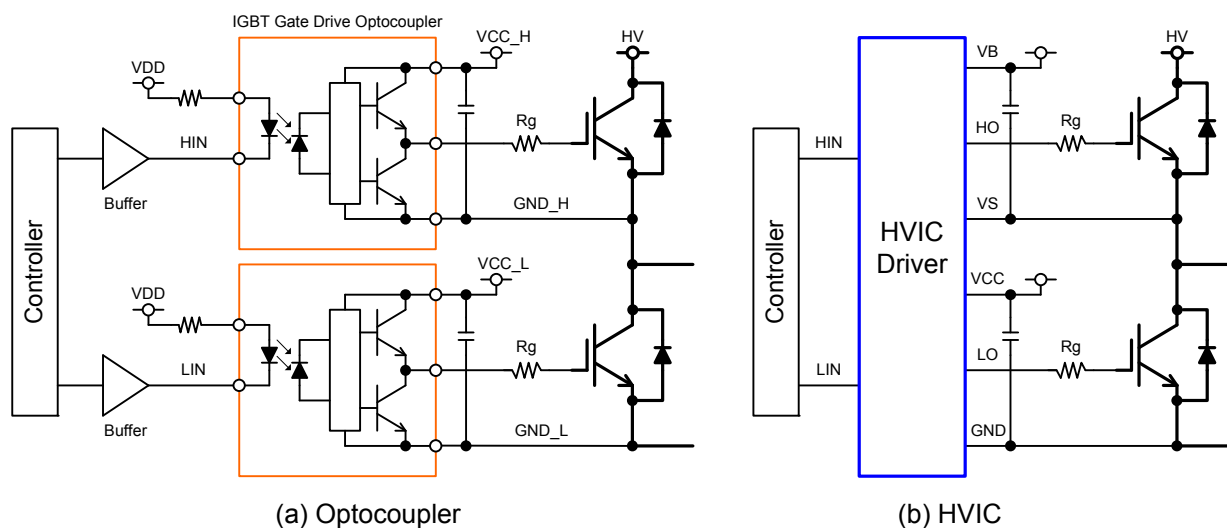


Figure 17. Typical drive circuit with optocoupler or HVIC

Item	Optocoupler*	HVIC (FA5650N)
Output current	-2.0A / +2.0A	-1.4A / +1.8A
Turn-on/off propagation delay	500ns (max)	170ns (max)
Propagation delay difference between turn-on and turn-off	450ns (max) tpHL-tpLH	90ns (max) ton-toff
Propagation delay difference between high and low side	250ns (max) tpHL (max)-tpHL (min)	30ns (max) ton(High-side)-ton(Low-side)
Dead time (depends on switching characteristics of power device)	Long (2~5us)	Short (under 1us)
Switching frequency	Low speed (50kHz)	High speed (500kHz)
Allowable offset supply voltage transient	15kV/us (CMR)	50kV/us
Allowable negative voltage on the floating terminal	Good	80V (typical value)
Negative gate bias	Easy	Additional circuit is necessary
Power supply current (without gate current)	IF=10mA Icc=2mA (Vo=OPEN) x2	IBS+ICC=0.67mA

*: Typical characteristics