Fuji Switching Power Supply Control IC

Green mode Quasi-resonant IC

FA5571/71A/72/73/74/ 5570/5671

Application Note

April 2011
Fuji Electric Co., Ltd.

Caution

1. The contents of this note (Product Specification, Characteristics, Data, Materials, and Structure etc.) were prepared in April 2011.
   The contents will subject to change without notice due to product specification change or some other reasons. In case of using the products stated in this document, the latest product specification shall be provided and the data shall be checked.

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4. Products described in this note are manufactured and intended to be used in the following electronic devices and electric devices in which ordinary reliability is required:
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   - Machine tool - Audio Visual equipment - Home appliance - Personal equipment
   - Industrial robot etc.

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   - Traffic signal equipment - Gas leak detector and gas shutoff equipment
   - Disaster prevention/Security equipment - Various equipment for the safety.

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   - Space equipment - Aircraft equipment - Atomic energy control equipment
   - Undersea communication equipment - Medical equipment.

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Contents

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- The contents of this note will subject to change without notice due to improvement.
- The application examples or the components constants in this note are shown to help your design, and variation of components and service conditions are not taken into account. In using these components, a design with due consideration for these conditions shall be conducted.

1. Overview

FA5571/71A/72/73/74/70/5671 is a quasi-resonant type switching power supply control IC with excellent stand-by characteristics. Though it is a small package with 8 pins, it has a lot of functions and enables to decrease external parts. Therefore it is possible to realize a small footprint and a high cost-performance power supply.

2. Features

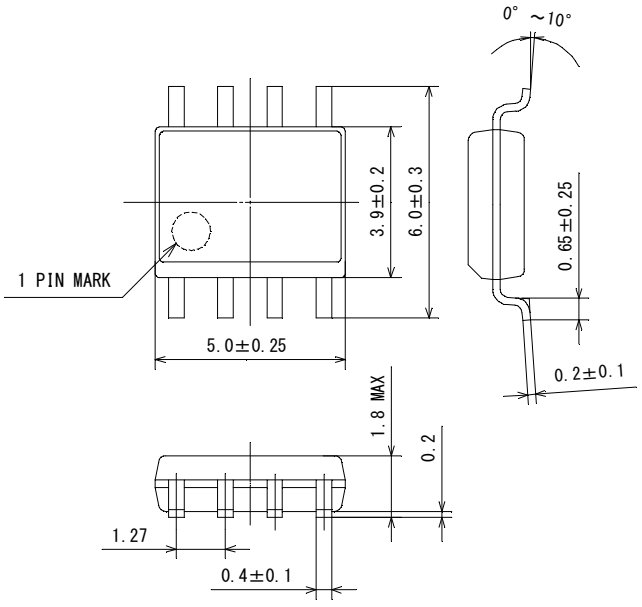
- A quasi-resonant type switching power supply.
- A power supply with excellent standby characteristics.
- Low power consumption with a built-in startup circuit.
- Low current consumption, in operation: 1.35mA
- Built-in maximum frequency limitation function: 120kHz(FA5571/72/73/74/70), 170kHz(FA5571A/5671)
- Operation at light load (FA5571/71A/72/70/5671: built-in burst function, FA5573/74: built-in frequency reduction function)
- Built-in drive circuit possible to connect to a power MOSFET directly. Output current: 0.5A (sink) 0.25A (source)
- Built-in overload protection function (FA5571/71A/73/70/5671: auto restart, FA5572/74: timer latch)
- Built-in latch protection function with the secondary over-voltage detection.
- Built-in transformer short circuit protection function.
- Built-in low voltage malfunction protection circuit.
- Package: SOP-8

Function list by types

Type	Overload protection	Light load operation	Maximum blanking frequency	ZCD pin timer latch Delay time T_{LAT1}	IS pin latch shutdown threshold	VCC pin OVP threshold	IS pin OCP threshold
FA5571	Auto restart	Burst	120kHz(TYP)	2.3us(TYP)	2.0V(TYP)	nonfunctional	1.0V(TYP)
FA5571A			170kHz(TYP)	4.5us(TYP)	2.0V(TYP)	nonfunctional	1.0V(TYP)
FA5570	Auto restart	Burst	120kHz(TYP)	nonfunctional	nonfunctional	nonfunctional	1.0V(TYP)
FA5671			170kHz(TYP)	nonfunctional	nonfunctional	28V(TYP)	0.5V(TYP)
FA5572	Timer latch	Burst	120kHz(TYP)	2.3us(TYP)	2.0V(TYP)	nonfunctional	1.0V(TYP)
FA5573	Auto restart	Frequency reduction	120kHz(TYP)	2.3us(TYP)	2.0V(TYP)	nonfunctional	1.0V(TYP)
FA5574	Timer latch	Frequency reduction	120kHz(TYP)	2.3us(TYP)	2.0V(TYP)	nonfunctional	1.0V(TYP)

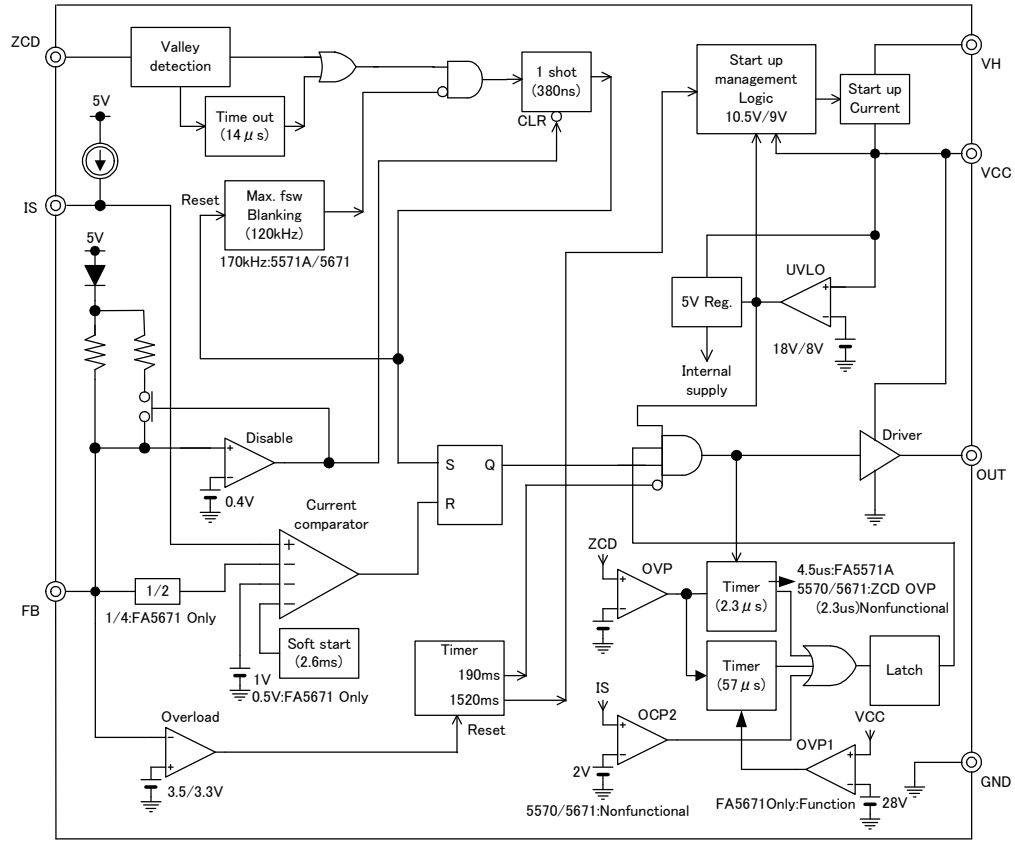
3. Outline drawings

SOP-8

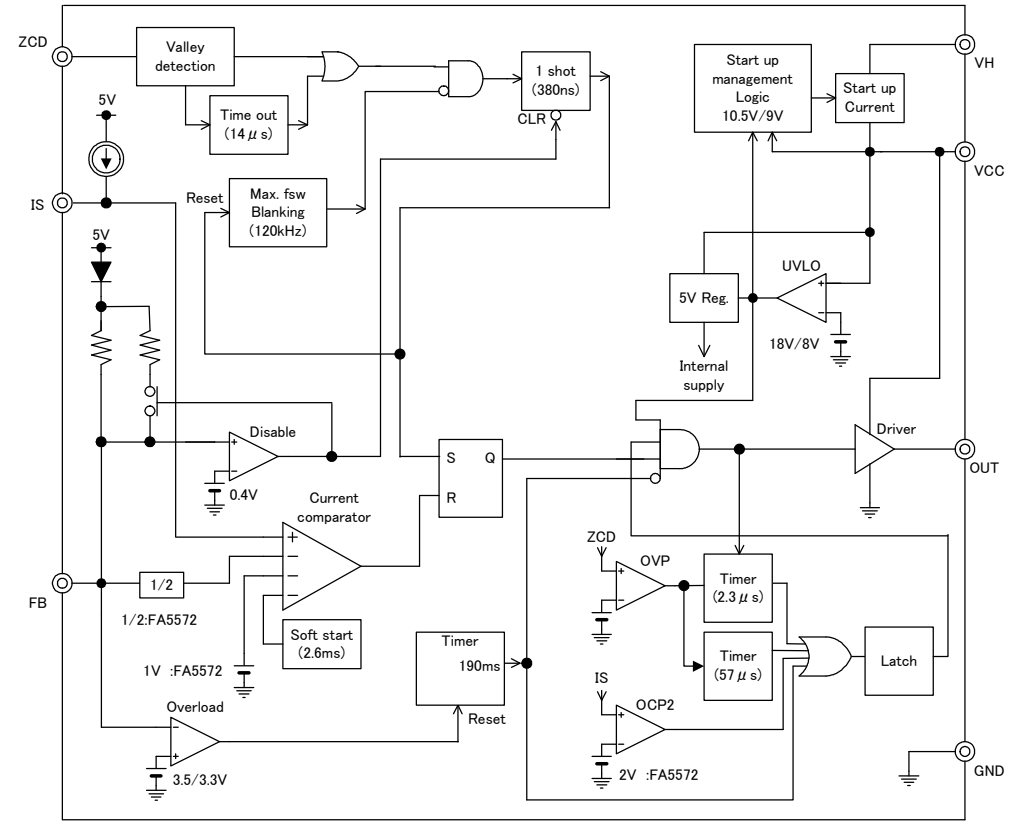


4. Block diagram

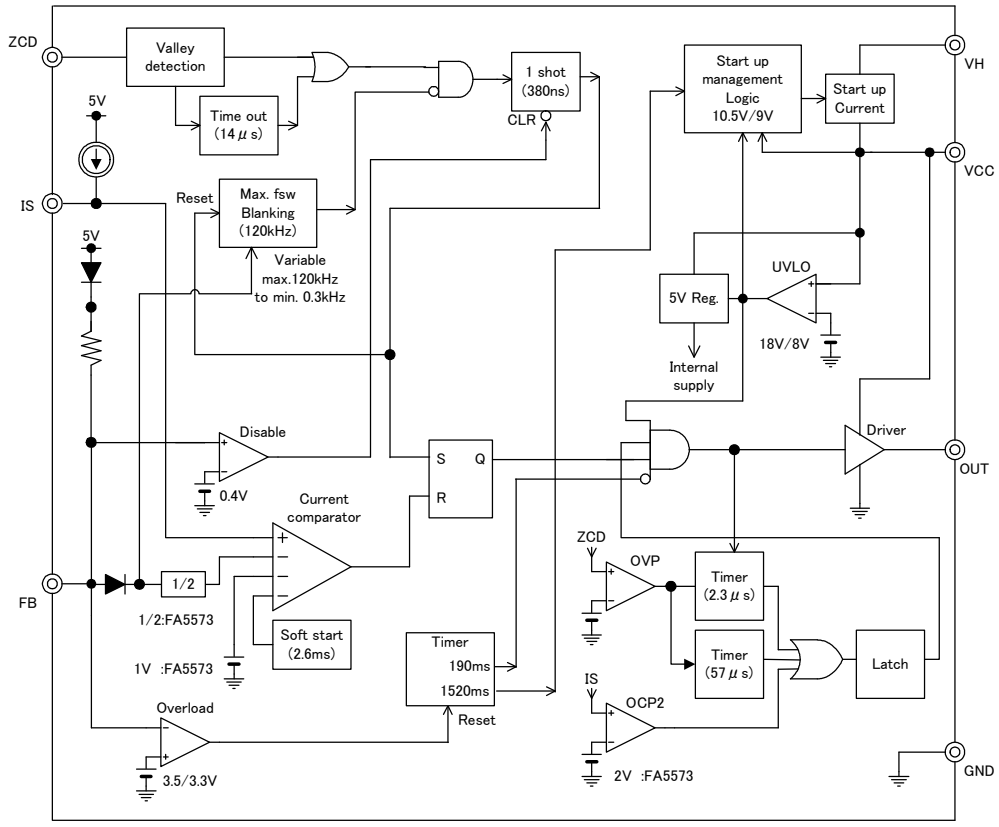
FA5571/71A/70/5671



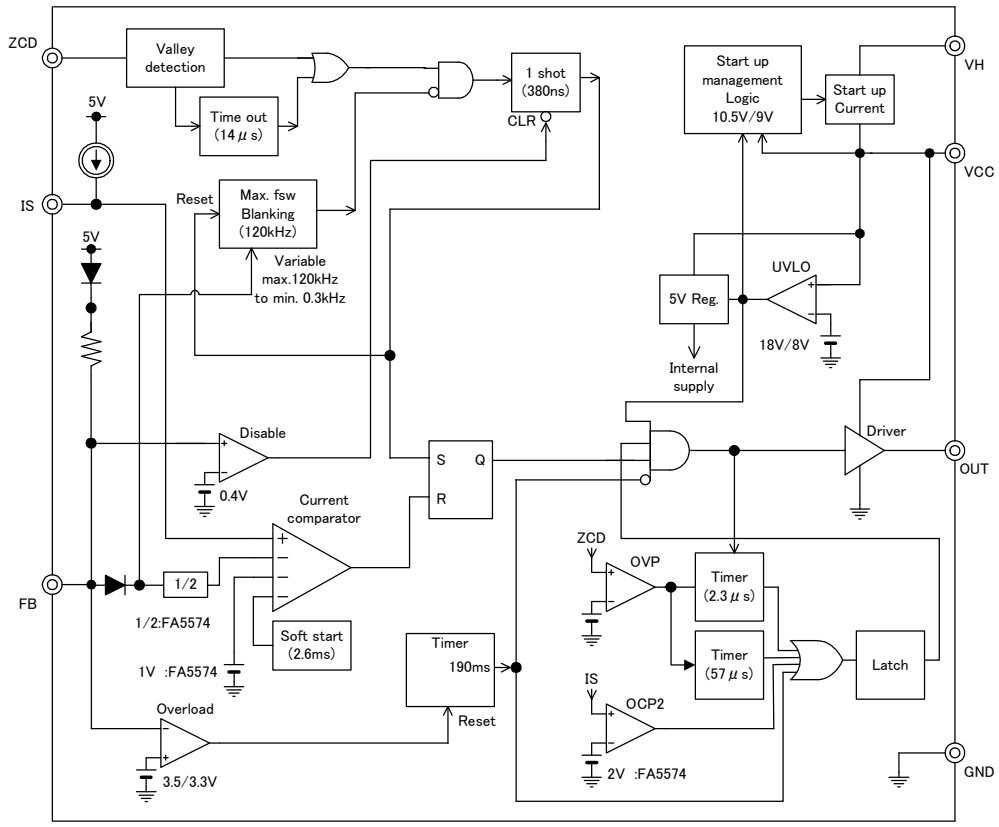
FA5572



FA5573



FA5574



5. Functional description of pins

Pin number	Pin name	Pin function
1	ZCD	Zero current detection input
2	FB	Feed-back input
3	IS	Current sense input
4	GND	Ground
5	OUT	Output
6	VCC	Power supply
7	NC	
8	VH	High voltage input

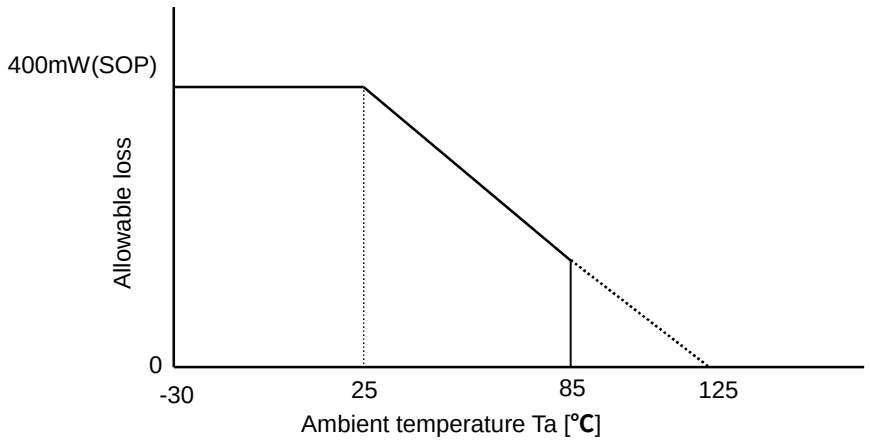
6. Rating and characteristics

* "+" shows sink and "–" shows source in current prescription.

(1) Absolute maximum rating

Item	Symbol	Rating	Unit
Power supply voltage	V_{CC}	30	V
OUT pin output peak current	I_{OH}	-0.25	A
	I_{OL}	+0.5	A
OUT pin voltage	V_{OUT}	-0.3 to VCC+0.3	V
FB, IS pin input voltage	V_{LT}	-0.3 to 5.0	V
ZCD pin current	I_{SOZCD}	-2.0	mA
	I_{SIZCD}	+3.0	
VH pin input voltage	VVH	-0.3 to 500	V
Total loss (Ta<25℃)	Pd	400 (SOP-8)	mW
Maximum junction temperature	Tj	125	℃
Storage temperature	Tstg	- 40 to +150	℃

* Allowable loss reduction characteristics



(2) Recommended operating condition

Item	Symbol	MIN	TYP	MAX	Unit
Power supply voltage(FA5571/ 71A/72/73/70)	Vcc	11	15	28	V
Power supply voltage(FA5671)		11	15	26	V
VH pin input voltage	VVH	80	-	450	V
VCC pin capacity	CVCC	10	47	220	μF
Operating ambient temperature	Ta	-40	-	85	℃

(3) Electric characteristics (Unless otherwise specified : Vcc=15V, Tj=25℃)

Current sensing part (IS pin)

Item	Symbol	Condition	MIN	TYP	MAX	Unit
Input bias current	I_{IS}	V_{IS}=0V	-60	-50	-40	μA
Maximum input threshold voltage	V_{thIS}	V_{FB}=3V, FA5571/71A/72 /73/74/70	0.9	1.0	1.1	V
		V_{FB}=3V, FA5671	0.45	0.5	0.55	V
Voltage gain	AV_{IS}	$\Delta V_{FB}/\Delta V_{IS}$	1.75	2.0	2.25	V/V
Minimum ON width	Tonmin	FB=3V, IS=1.5V	260	380	500	ns
Output delay time *1	T_{pdIS}	IS input: 0V to 1.5V (Pulse signal)	100	175	320	ns
Latch shutdown threshold voltage	VthISat		1.8	2.0	2.2	V

Feedback part (FB pin)

Item	Symbol	Condition	MIN	TYP	MAX	Unit
Pulse shutdown FB pin voltage	V_{THFB0}	Duty cycle=0%	340	400	460	mV
FB pin input resistance	R_{FB}	FA5571/71A/72/70/5671 V_{FB}=1V to 2V	14.4	18.0	21.6	kΩ
		FA5573/74 V_{FB}=1V to 2V	17.6	22.0	26.4	kΩ
FB pin current	I_{FB0}	V_{FB}=0V	-240	-200	-160	μA
FB pin threshold voltage for light load mode	V_{FBM}	FA5573/74	0.95	1.15	1.35	V
Minimum oscillation frequency	F_{min}	FA5573/74 V_{FB}=0.5V	0.15	0.3	0.4	kHz

Zero current detection part (ZCD pin)

Item	Symbol	Condition	MIN	TYP	MAX	Unit
Input threshold voltage	V_{THZCD1}	V_{ZCD} decreasing	40	60	100	mV
	V_{THZCD2}	V_{ZCD} increasing	150	250	340	mV
Hysteresis width	V_{HYZCD}		110	190	240	mV
Input clamp voltage	V_{IH}	I_{ZCD}=+3mA (High state)	8.2	9.2	10.2	V
	V_{IL}	I_{ZCD}=-2mA (Low state)	-0.93	-0.8	-	V
ZCD delay time *1	T_{ZCD}		-	155	300	ns
Maximum blanking frequency	F_{max}	FA5571/72/73/74/70	108	120	140	kHz
		FA5571A/5671	155	170	185	kHz
Timeout period from the last ZCD trigger *1	T_{OUT}		10	14	18	μs
ZCD pin internal resistance	Rzcd		22.5	30	37.5	kΩ

Over-voltage protection part (ZCD pin)

Item	Symbol	Condition	MIN	TYP	MAX	Unit
ZCD pin over-voltage threshold level	V_{OVP}		6.4	7.2	8.0	V
VCC pin over-voltage threshold level	V_{OVP1}	FA5671	26	28	30	V
Timer latch delay time *1	T_{LAT1}	Delay from turn-off FA5571/72/73/74	1.8	2.3	2.8	µs
		Delay from turn-off FA5571A	3.5	4.5	5.5	µs
	T_{LAT2}	Delay from exceeding the Vovp voltage	40	57	75	µs

Overload protection part (FB pin)

Item	Symbol	Condition		MIN	TYP	MAX	Unit
FB pin overload detection threshold level *1	V_{OLP1}	VFB increasing		3.3	3.5	3.8	V
	V_{OLP2}	VFB decreasing		3.0	3.3	3.6	V
OLP delay time	T_{OLP}	FA5571/71A/73/70/5671 : Switching continuing time after detecting overload. FA5572/74 : Timer latch delay time after detecting overload.		133	190	247	ms
OLP output shutdown time *1	T_{OFF}	Switching shutdown time after T_{OLP} period	FA5571/ 71A/73/70/ 5671	930	1330	1730	ms

Soft start part

Item	Symbol	Condition	MIN	TYP	MAX	Unit
Soft start time *1	T_{SFT}		1.6	2.6	3.6	ms

Output part (OUT pin)

Item	Symbol	Condition	MIN	TYP	MAX	Unit
L output voltage	V_{OL}	I_{OL}=100mA VCC=15V	0.5	1.0	2.0	V
H output voltage	V_{OH}	I_{OH}=-100mA V_{CC}=15V	12	13.2	14.5	V
Rise time *1	tr	CL=1nF, Tj=25°C	20	40	100	ns
Fall time *1	tf	CL=1nF, Tj=25°C	15	30	70	ns

High voltage input part (VH pin)

Item	Symbol	Condition	MIN	TYP	MAX	Unit
VH pin input current	I_{VHrun}	V_{VH}=400V, V_{CC}>V_{STOFF}	10	30	60	μA
	I_{VH1}	V_{CC}=6.5V, V_{VH}=100V Tj=25°C	4.0	6.8	9.6	mA
	I_{VH0}	V_{CC}=0V, V_{VH}=100V Tj=25°C	0.8	1.6	2.5	mA
VCC pin charging current	I_{pre1}	V_{CC}=8V, V_{VH}=100V Tj=25°C	-9	-6.4	-3.7	mA
	I_{pre2}	V_{CC}=16V, V_{VH}=100V Tj=25°C	-8	-4.8	-3	mA

Low voltage malfunction protection circuit (UVLO) part (VCC pin)

Item	Symbol	Condition	MIN	TYP	MAX	Unit
ON threshold voltage	V_{CCON}	UVLO	16	18	20	V
OFF threshold voltage	V_{CCOFF}	UVLO	7	8	9	V
Hysteresis width	V_{HYS1}		8	10	12	V
Startup current shutdown voltage	V_{STOFF}	Vcc increasing	9.5	10.5	12	V
Startup current reset voltage	V_{STRST1}	Vcc decreasing	8	9	10	V
Hysteresis width (startup current)	V_{HYS2}		0.5	1.5	2.0	V

Current consumption (VCC pin)

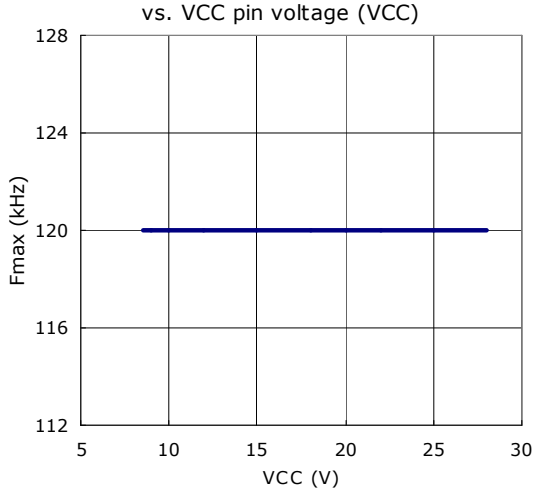
Item	Symbol	Condition	MIN	TYP	MAX	Unit
Power supply current in operation	I_{CCOP1}	VFB=2.5V、VIS＝1.5V、VZCD=0V、OUT=no_load	0.9	1.35	2.0	mA
	I_{CCOP2}	Duty cycle=0%, VFB=0V	0.9	1.33	1.9	mA
Power supply current at latch	I_{CClat}	FB=open VCC=11V	350	500	650	μA

*1 : Regarding to these items, 100% test is not carried out. A specified value is a design guarantee.
The column showing '-' has no specified value.

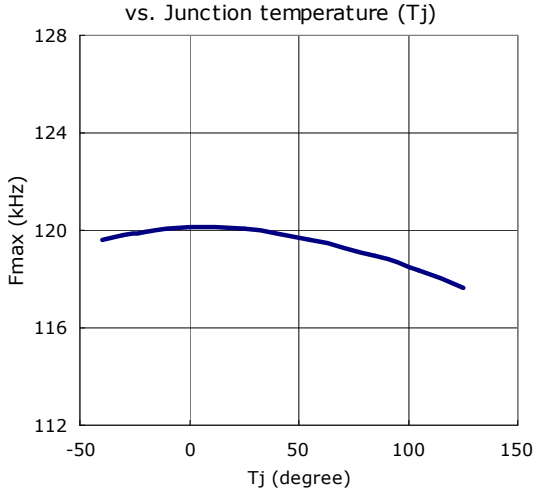
7. Characteristic curve

- Unless otherwise specified : Ta=25℃, VCC=15V(*FA5571)
- “+” shows sink and “–“ shows source in current prescription.
- Data listed here shows the typical characteristics of an IC and does not guarantee the characteristics.

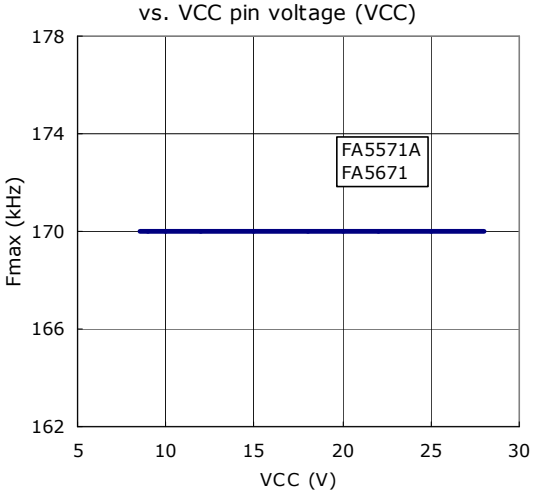
Maximum fsw blanking (Fmax)
vs. VCC pin voltage (VCC)



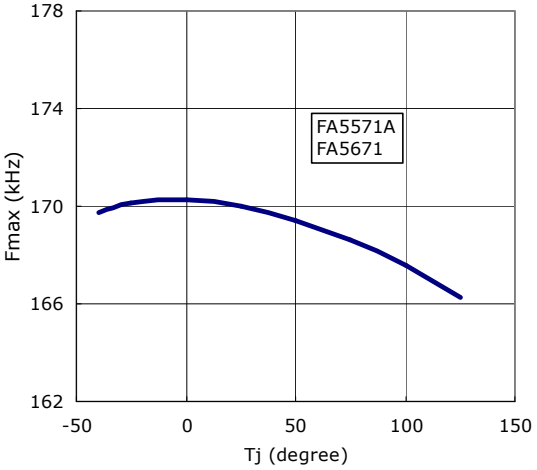
Maximum fsw blanking (Fmax)
vs. Junction temperature (Tj)



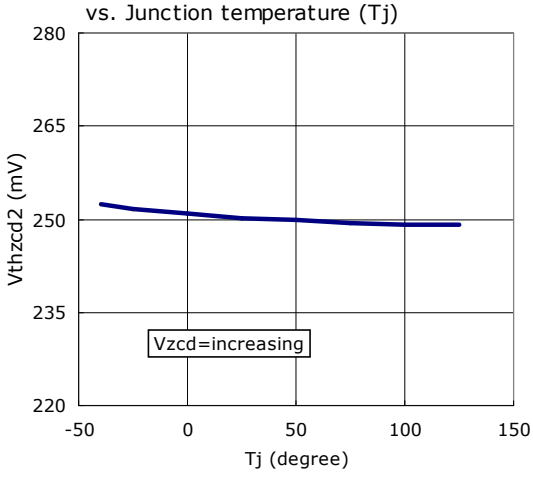
Maximum fsw blanking (Fmax)
vs. VCC pin voltage (VCC)



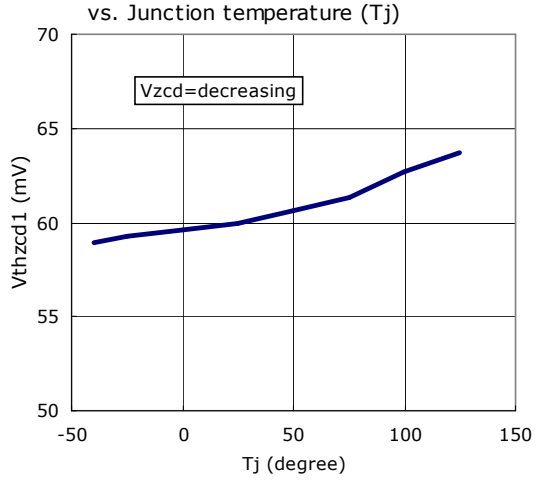
Maximum fsw blanking (Fmax)
vs. Junction temperature (Tj)



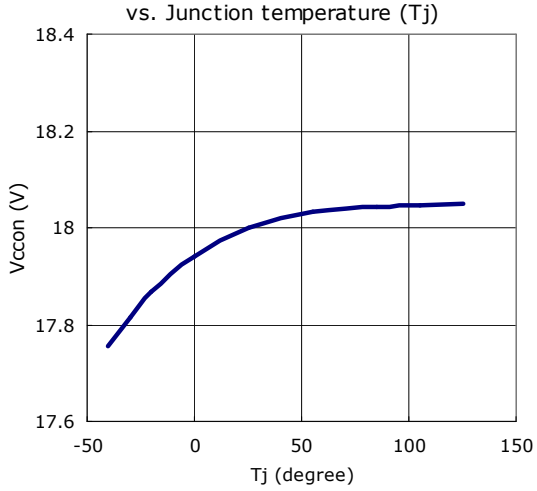
ZCD pin input threshold voltage
(Vthzcd2)
vs. Junction temperature (Tj)



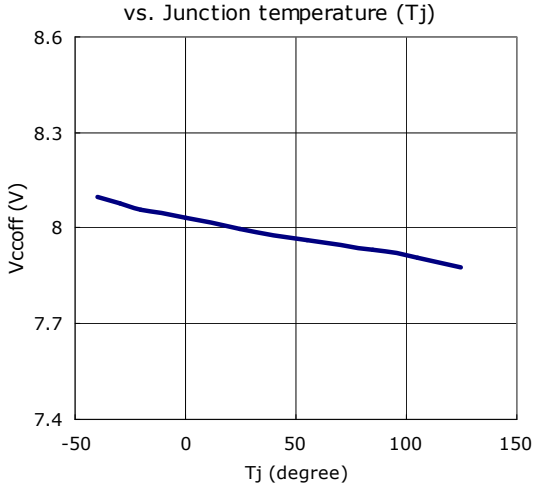
ZCD pin input threshold voltage
(Vthzcd1)
vs. Junction temperature (Tj)



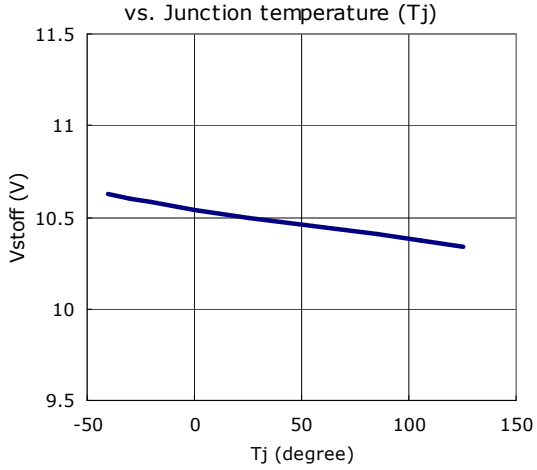
UVLO ON threshold voltage (Vccon)
vs. Junction temperature (Tj)



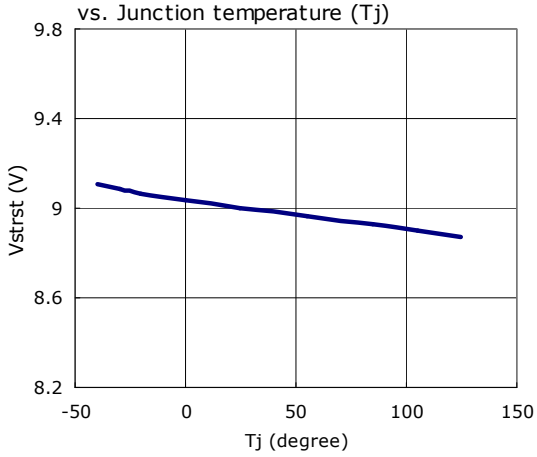
UVLO OFF threshold voltage (Vccoff)
vs. Junction temperature (Tj)



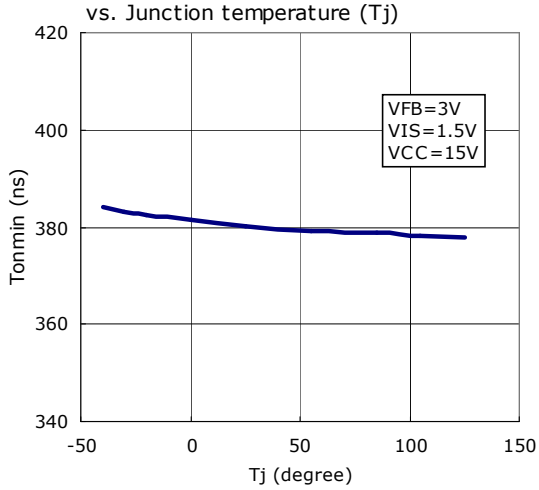
Start-up circuit off threshold voltage
(Vstoff)
vs. Junction temperature (Tj)



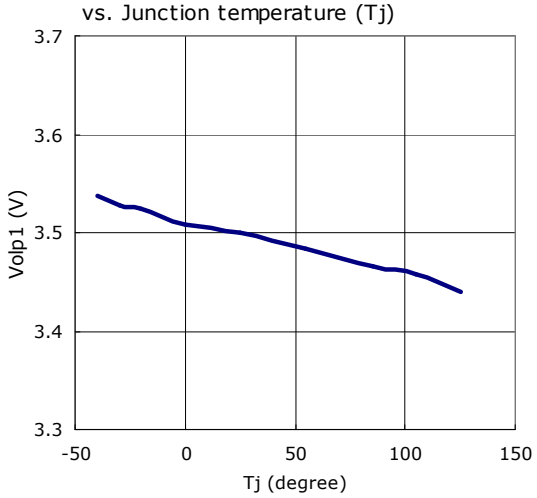
Start-up circuit restart threshold
voltage (Vstrst)
vs. Junction temperature (Tj)



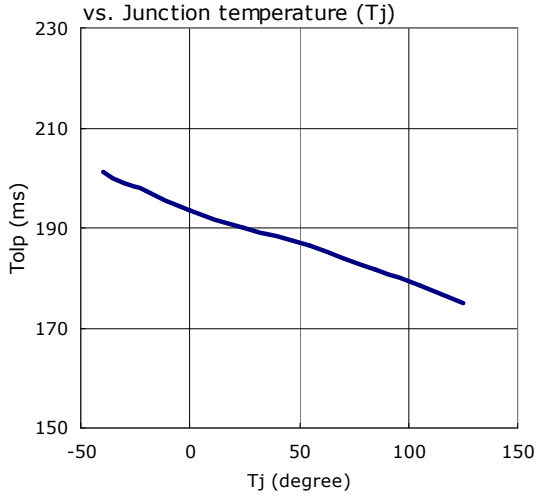
Minimum ON width (Tonmin)
vs. Junction temperature (Tj)



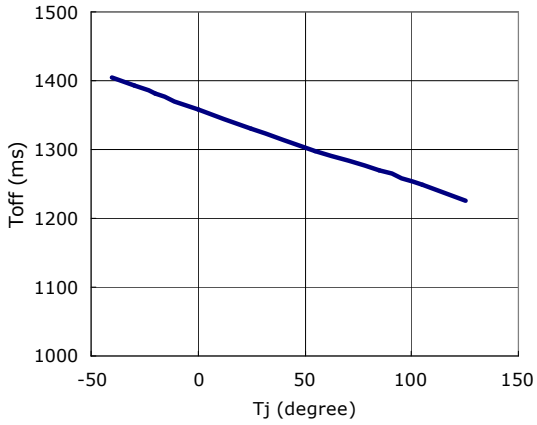
OLP threshold voltage (Volp1)
vs. Junction temperature (Tj)



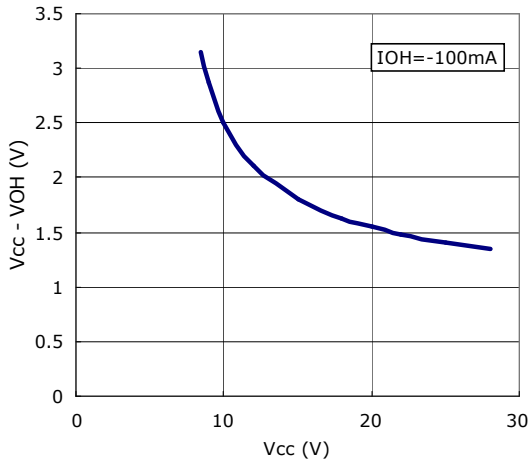
Delaytime to OLP (Tolp)
vs. Junction temperature (Tj)



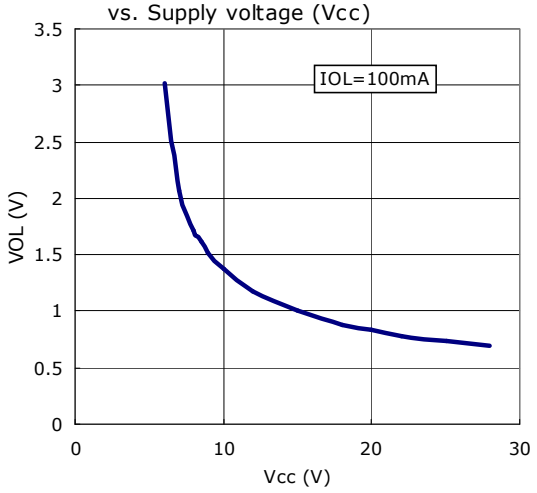
OLP offtime (Toff)
vs. Junction temperature (Tj)



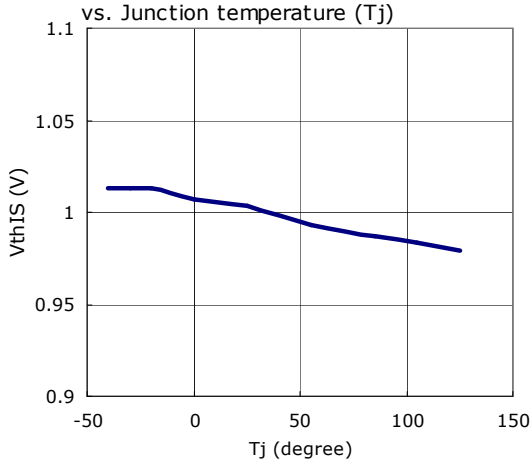
High output voltage (VOH)
vs. Supply voltage (Vcc)



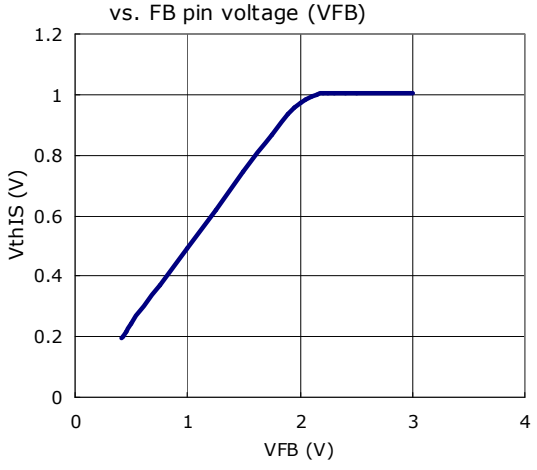
Low output voltage (VOL)
vs. Supply voltage (Vcc)



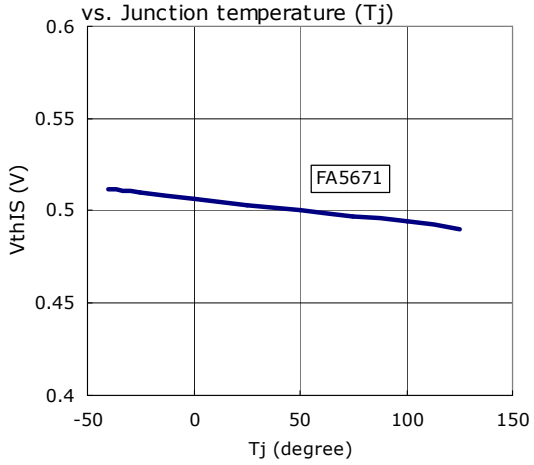
IS pin maximum threshold voltage
(VthIS)
vs. Junction temperature (Tj)



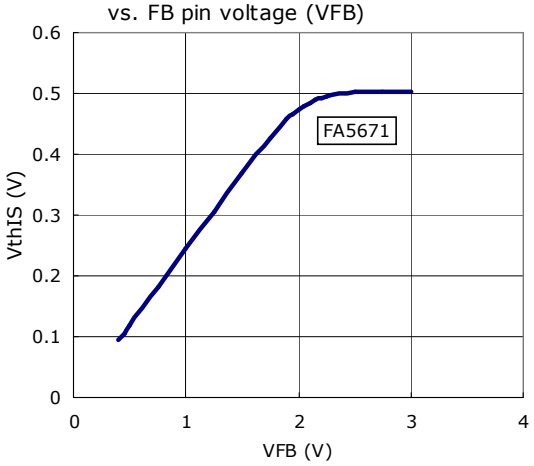
IS pin maximum threshold voltage
(VthIS)
vs. FB pin voltage (VFB)



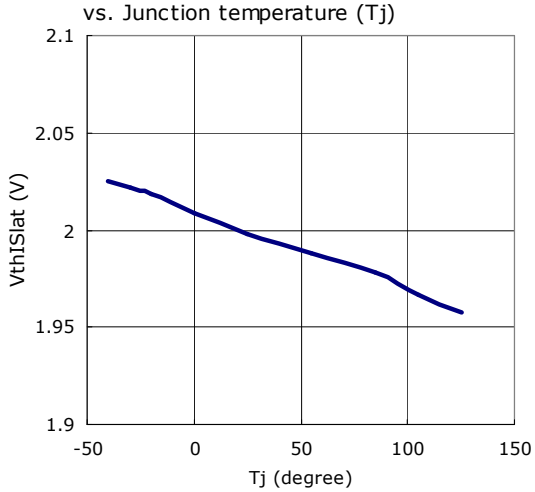
IS pin maximum threshold voltage (VthIS) vs. Junction temperature (Tj)



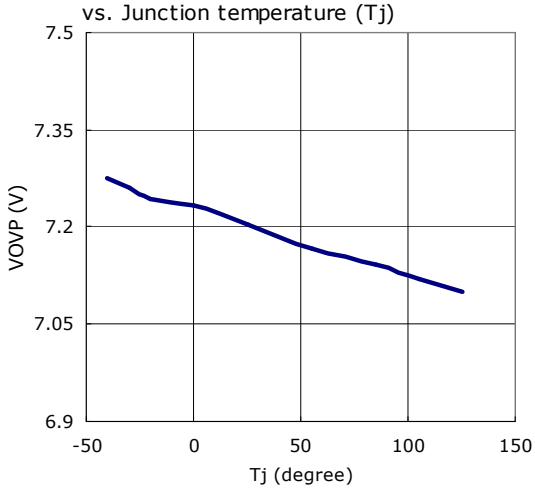
IS pin maximum threshold voltage (VthIS) vs. FB pin voltage (VFB)



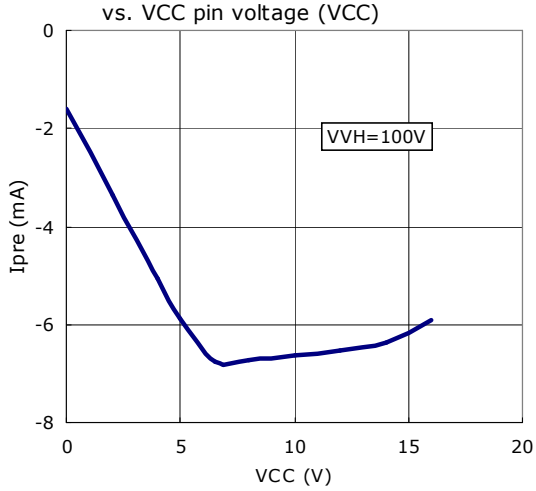
IS pin latch threshold voltage (VthISlat) vs. Junction temperature (Tj)



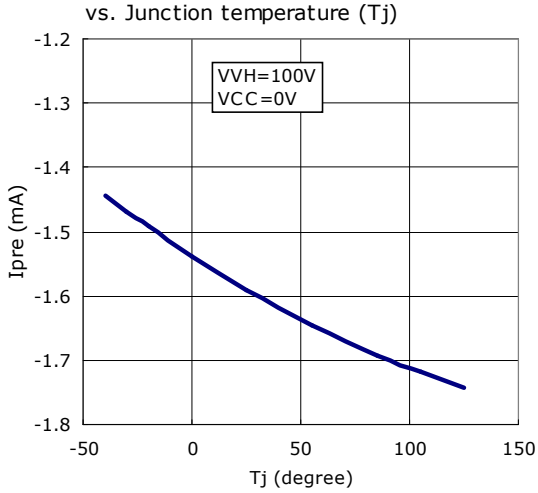
ZCD pin OVP threshold voltage (VOVP) vs. Junction temperature (Tj)



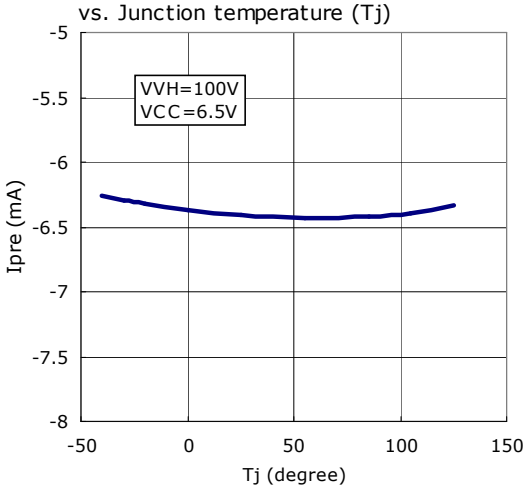
Charge current for VCC pin (Ipre) vs. VCC pin voltage (VCC)



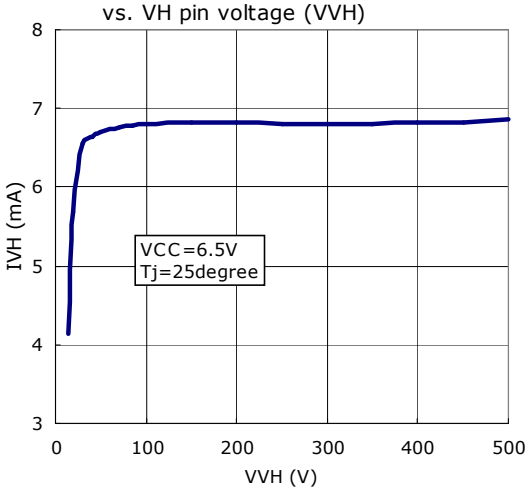
Charge current for VCC pin (Ipre) vs. Junction temperature (Tj)



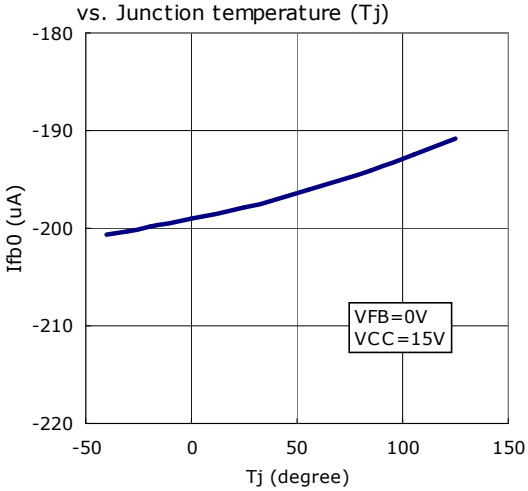
Charge current for VCC pin (Ipre)
vs. Junction temperature (Tj)



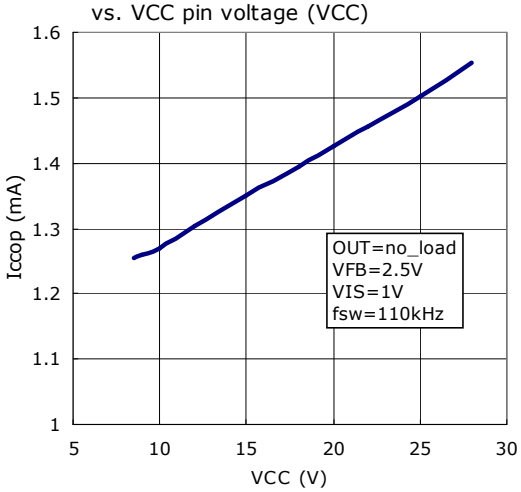
VH pin input current (Ipre)
vs. VH pin voltage (VVH)



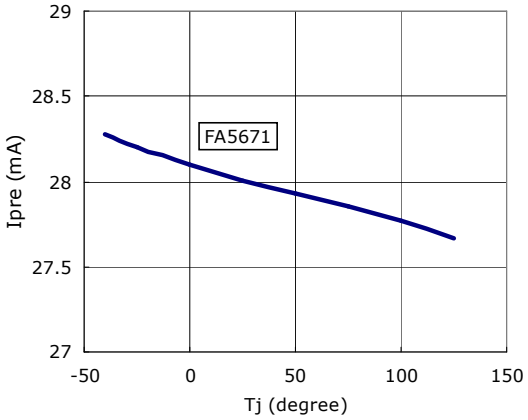
FB pin source currnt (Ifb0)
vs. Junction temperature (Tj)



Operating-state supply current (Iccop)
vs. VCC pin voltage (VCC)



VCC pin OVP threshold Voltage(Vovp1)
vs. Junction temperature (Tj)



8. Basic operation

The basic operation of the power supply using IC is not switching operation with fixed frequency using an oscillator but switching with self-excited oscillation. This is shown in Fig.1 Schematic circuit diagram and Fig.2 Waveform in the basic operation.

t1 to t2

Q1 turns ON and then Q1 drain current Id (primary current of T1) begins to rise from zero. Q1 current is converted into the voltage by Rs and is input into IS pin.

t2

When the current of Q1 get to the reference voltage of the current comparator that is fixed by the voltage of FB pin, a reset signal is input into RS flip-flop and Q1 turns OFF.

t2 to t3

When Q1 turns OFF, then the coil voltage of the transformer turns over and the current IF is provided from the transformer into the secondary side through D1.

t3 to t4

When the current from the transformer into the secondary side stops and the current of D1 gets to zero, the voltage of Q1 turns down rapidly due to the resonance of the transformer inductance and the capacitor Cd. At the same time the transformer auxiliary coil voltage Vsub also drops rapidly.

ZCD pin receives this auxiliary coil voltage but then it has a little delay time because of CR circuit composed with RZCD and CZCD on the way.

t4

If ZCD pin voltage turns down lower than the threshold voltage (60mV(typ.)) of Valley detection, a set signal is input into R-S flip-flop and Q1 turns ON again. If the delay time of CR circuit placed between the auxiliary coil and ZCD pin is adjusted properly, Q1 voltage can be turned on at the bottom. This operation makes the switching loss of TURN ON to the minimum.

(Return to t1)

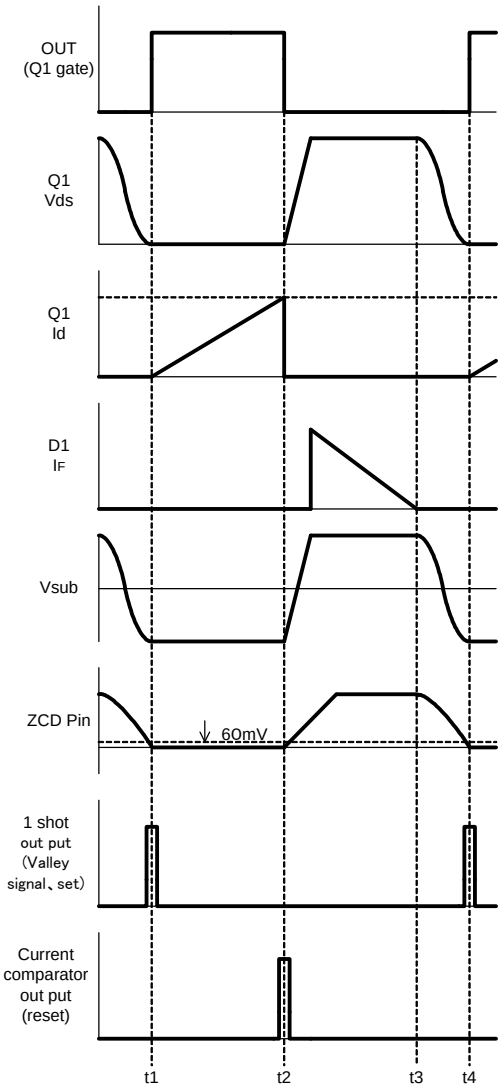


Fig.2 Waveform in basic operation

Subsequently repeat from t1 to t4 and continue switching.

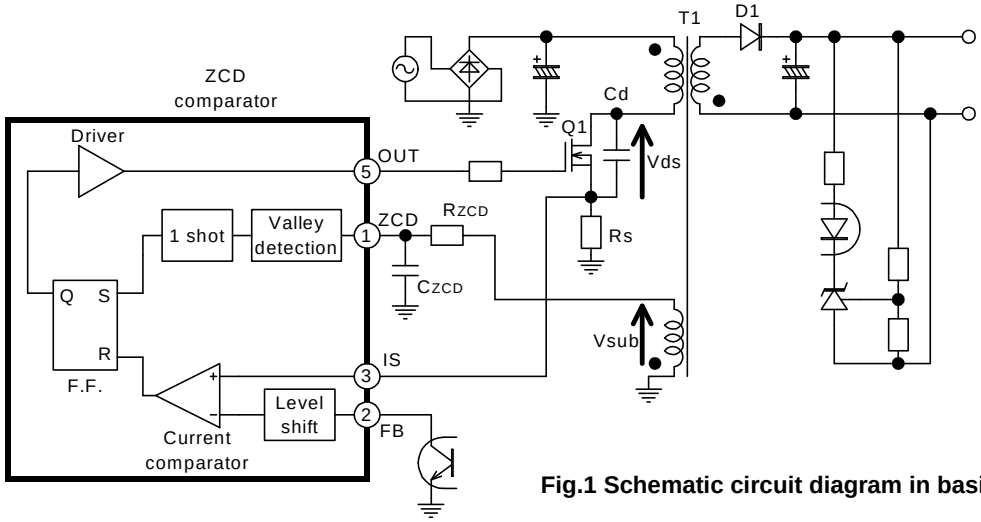


Fig.1 Schematic circuit diagram in basic operation

9. Description of the function

(1) Steady- state operation and burst operation at light load (FA5571/72/70)

FA5571A/5671 Maximum blanking frequency : 170kHz

・ **Steady- state operation**

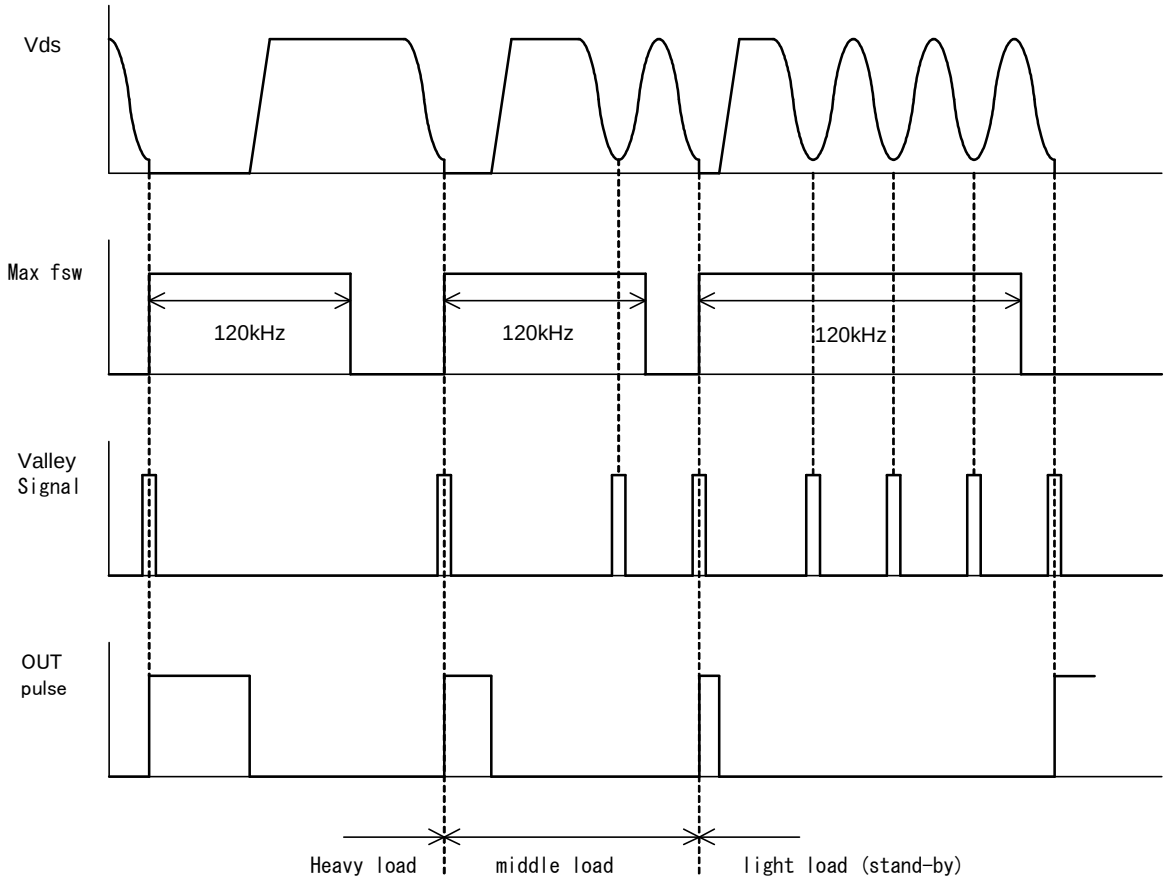


Fig.3 Steady-state operation timing chart

At each switching cycle, TURN ON is carried out at the first Valley signal that exceeds the time corresponding to the maximum frequency limit of 120kHz (170kHz : 5571A/5671), counting from the previous TURN ON.

・ **Burst operation at light load**

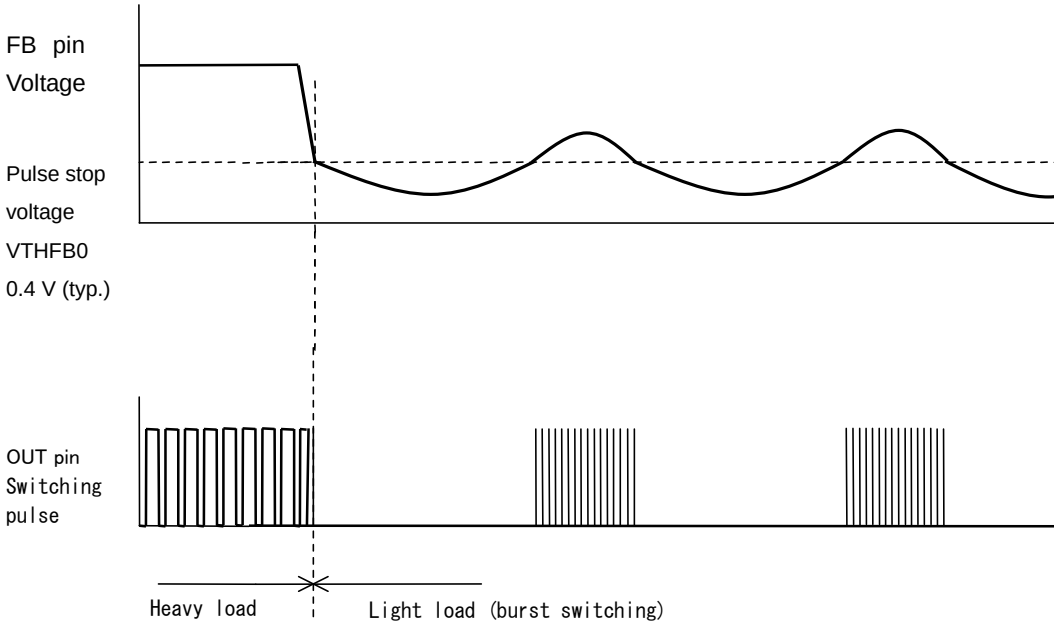


Fig.4 Burst operation at light load

When FB pin voltage drops lower than the pulse shutdown threshold voltage, switching is shut down. On the contrary when FB pin voltage rises higher than the pulse shutdown threshold voltage, switching is started again. FB pin voltage overshoots and undershoots centering around the pulse shutdown threshold voltage for mode change. Continuous pulse is output during the overshoot period and long period burst frequency is obtained during the undershoot period.

(2) Steady-state operation and frequency reduction operation at light load (FA5573/74)

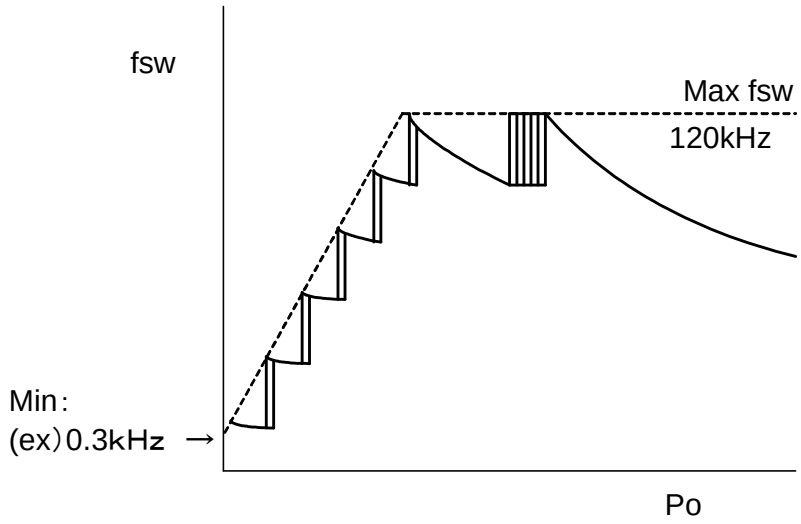


Fig. 5 Oscillation frequency (f sw) vs output power characteristics (Po)

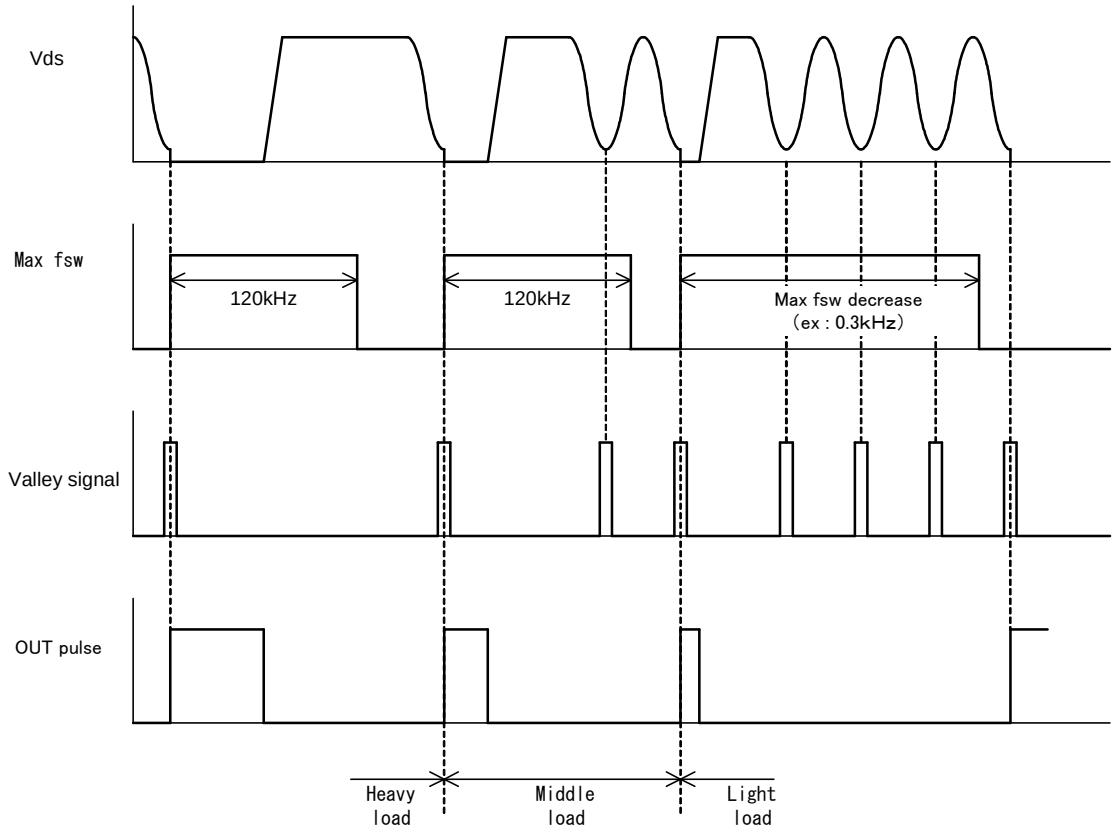


Fig.6 Steady-state operation timing chart

In the normal operation, each switching cycle is turned on at the first valley signal beyond the time corresponding to the maximum frequency limitation of 120 kHz after the previous turn-on. Moreover, in the light load operation, the maximum frequency limitation is decreased. The frequency lowers approximately to 0.3 kHz at minimum.

(3) Startup circuit and auxiliary coil voltage

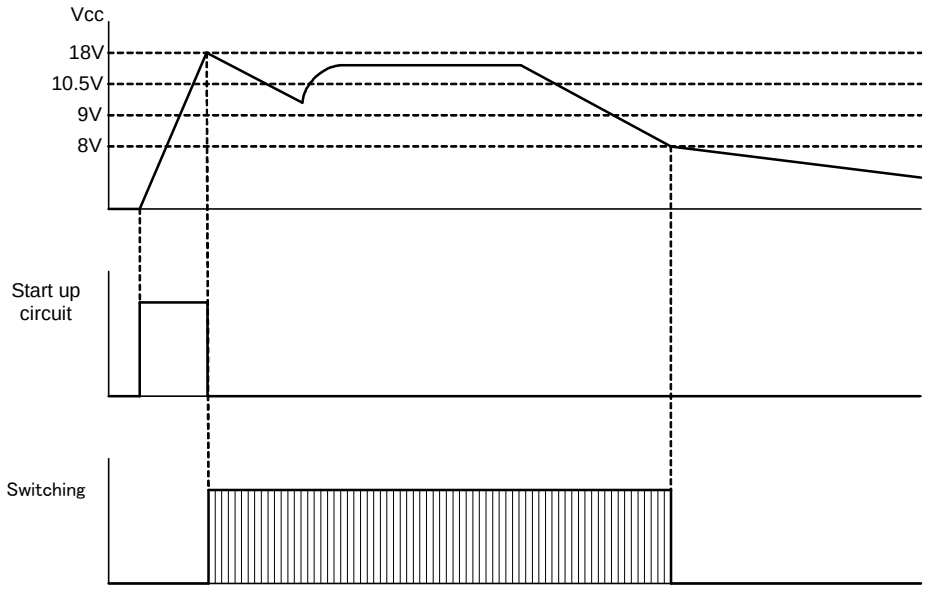


Fig.7 Startup and shutdown (the auxiliary coil voltage is higher than 9 V)

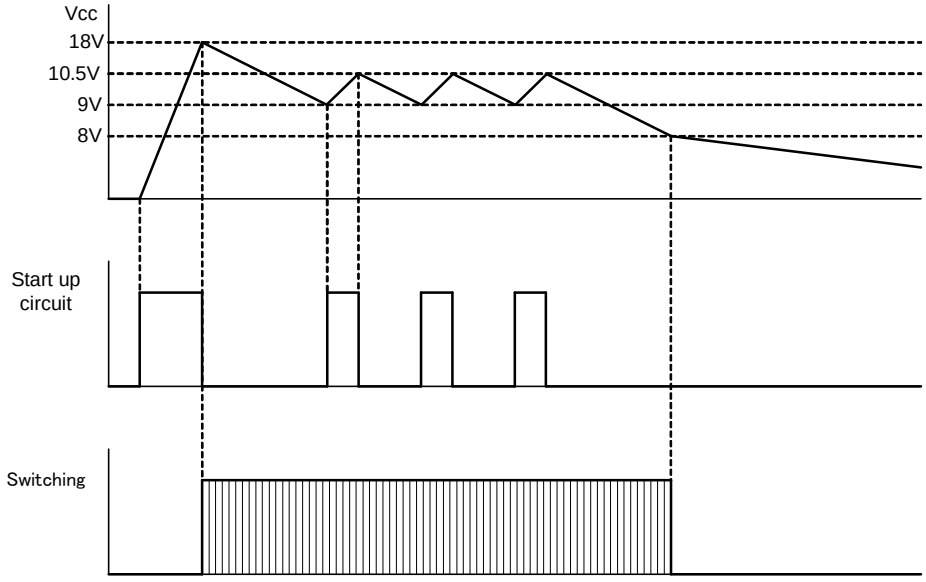


Fig.8 Startup and shutdown (the auxiliary coil voltage is lower than 9 V)

If the auxiliary coil voltage is higher than 9V, the startup circuit operates only at the startup and since then operates being provided with the auxiliary coil voltage as a power supply.

While the auxiliary coil voltage is lower than 9V, the startup circuit continues to keep Vcc between 9V and 10.5V by ON-OFF.

(4) Operation at overload

■**FA5571/71A/73/70/5671 (Auto restart type)**

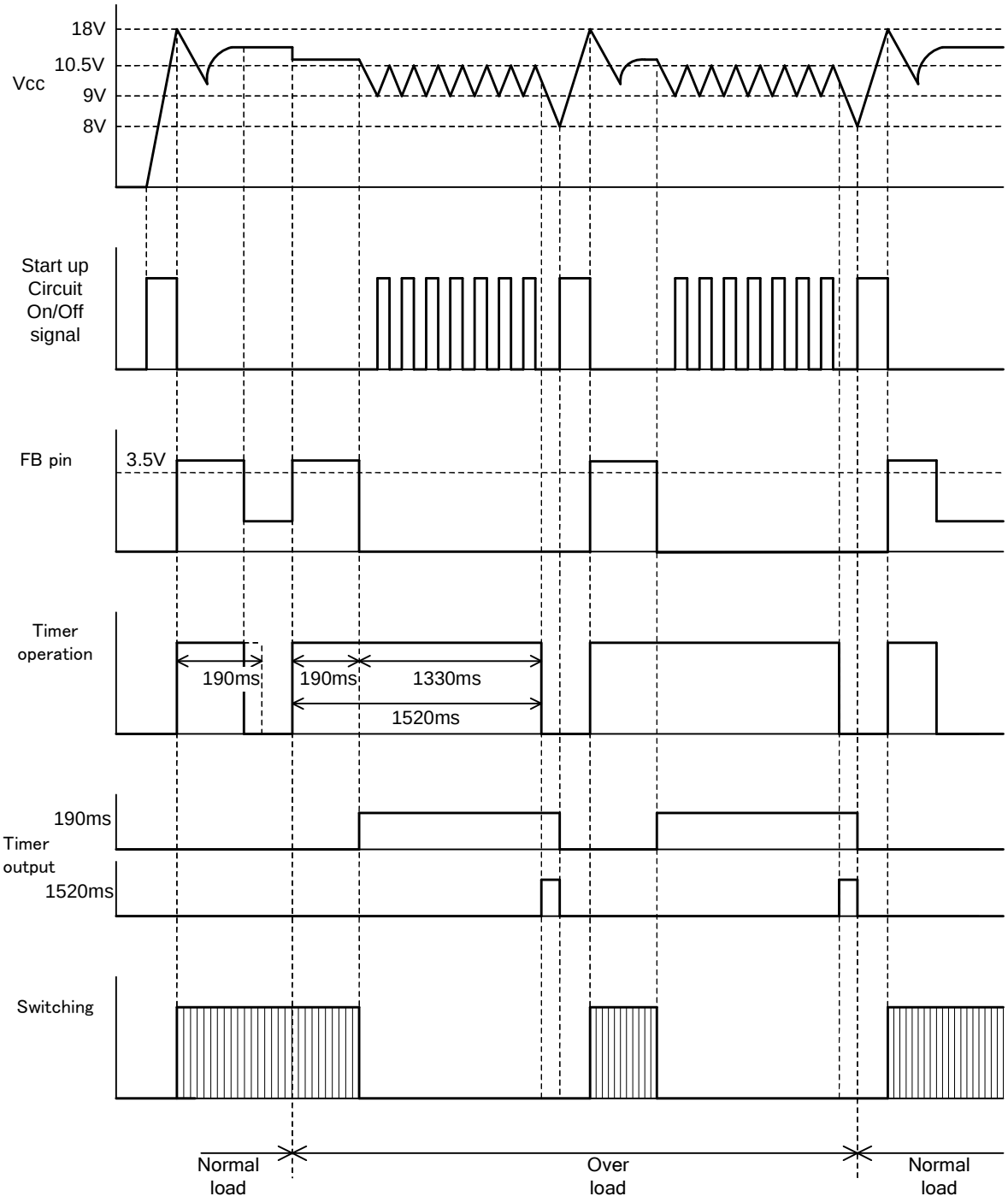


Fig.9 Operation at overload (FA5571/71A/73/70/5671)

If the overload condition continues longer than 190ms, switching is forced to shut down using an internal timer.
The startup circuit is possible to operate within 1520ms after the beginning of the overload condition.
If the overload condition continues, switching is done for 190ms and after then Vcc is provided with the startup circuit for 1330ms and the operation shutdown condition is maintained.
When 1520ms passes after the beginning of the overload condition, a startup circuit stops its operation and Vcc begins to decrease. When Vcc gets down to 8.0V, the IC is once reset and restarted. Since then startup and shutdown are repeated if the overload condition continues. If the load returns to normal, the IC returns to the normal operation.
Even then, the output voltage must rise up to the setting value at the startup within 190ms settled with a timer.

■FA5572/74(latch type)

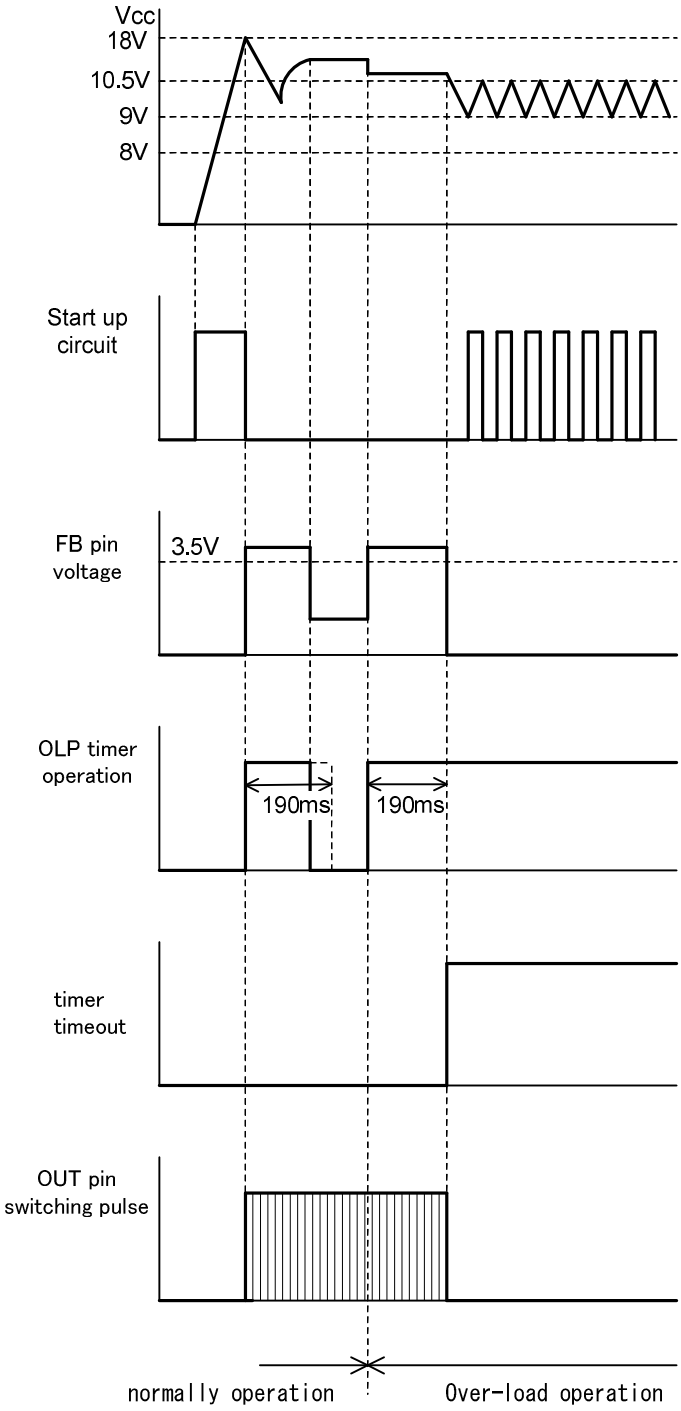


Fig.10 Operation at overload (FA5572/74)

If the overload condition continues longer than 190ms, switching is forced to shut down using an internal timer, and changes to latch mode to maintain this condition. During the condition when switching is shut down due to an overload latch, Vcc is provided with the startup circuit and the operation shutdown condition is maintained.

To reset the overload latch, shut down the supply of Vcc from the startup circuit by stopping the input voltage and reduces Vcc lower than 8.0V, the OFF-threshold voltage.

Even then, the output voltage must rise up to the setting value at the startup within 190ms settled with a timer.

(5) Others

・By pulling-up ZCD pin voltage higher than 7.2V from the outside, shutdown can be carried out. This condition is maintained until the input voltage is shut down and Vcc drops to the OFF threshold voltage of UVLO.

・Automatic reset with overload protection

If Vcc is provided by other power supply, latch-stop is carried out.

10. Direction for use of pins

(1) No.1 pin (ZCD)

Function

(**i**) Detection of timing to make a MOSFET turn ON.

(**ii**) Latch protection with an external signal.

(**iii**) Latch protection for over-voltage on the secondary side.

Usage

(i) Detection of turn-on timing

・Connection

This pin is connected to a transformer auxiliary winding through CR circuit with RZCD and CZCD. (Fig.11) Be careful about polarity of an auxiliary winding.

・Operation

When ZCD pin voltage drops lower than 60mV, MOSFET is turned on.

The auxiliary winding voltage swings + and – direction widely along with switching. A clamp circuit is equipped to protect IC from this voltage. If the auxiliary winding voltage is plus, it passes a current shown in Fig. 12 and if minus, shown in Fig.13. And then it clamps ZCD pin voltage.

・Complement

Since the threshold voltage of latch protection by an external signal is 6.4V (min.) as described in function (ii), the resistor RZCD must be adjusted for ZCD pin voltage not to exceed 6.4V in ordinary operation. At the same time the resistor RZCD must be adjusted for ZCD pin current not to exceed the absolute maximum rating.

The MOSFET voltage oscillates just before TURN ON due to the resonance effect between transformer inductance and resonant capacitor Cd. CZCD is adjusted for MOSFET to turn on at the bottom of this resonance (Fig.14). Generally RZCD is several 10kΩ and CZCD is several 10pF. However CZCD is unnecessary if good timing is obtained.

(**ii**) Latch protection with an external signal

▪ Connection

Pull up ZCD pin by an external signal.

A connection example in case of over-voltage on the primary side is shown in Fig.15. (Constants are examples. Check the behavior in actual circuit.)

▪ Operation

If ZCD pin voltage exceeds 7.2V (typ.) and this condition continues longer than 57μs(typ.), latch protection is carried out.

Once latch protection is carried out, the output pulse of the IC is shut down and this condition is maintained.

Reset is done by decreasing Vcc lower than UVLO off-threshold voltage.

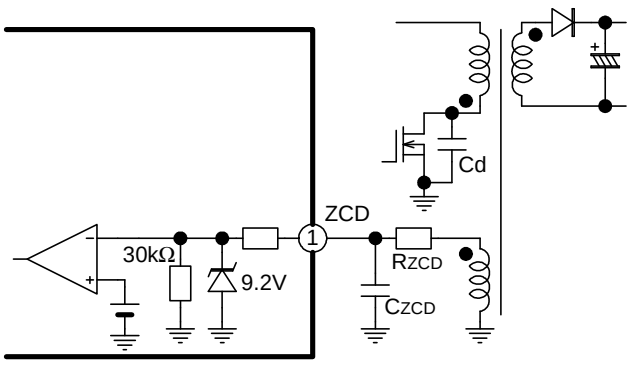


Fig.11 ZCD pin circuit

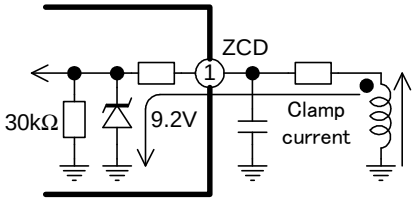


Fig.12 Clamping circuit (auxiliary coil voltage is plus)

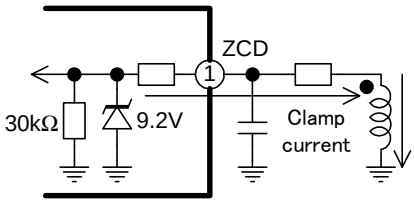


Fig.13 Clamping circuit (auxiliary coil voltage is minus)

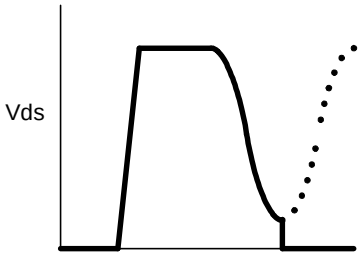


Fig.14 Vds waveform

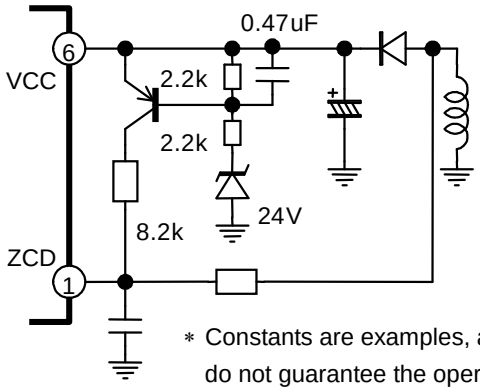


Fig.15 Over-voltage protection circuit for the primary side

(**iii**) Latch protection for over-voltage on the secondary side

▪ Connection (FA5571/71A/72/73/74)

Same as (**i**) Detection of turn-on timing.

▪ Operation

If the secondary output voltage (Vo) gets to the over-voltage, the auxiliary coil voltage and ZCD pin voltage also rise.

When ZCD pin voltage exceeds 7.2V (typ.) and 2.3 uS (typ.) (71A：4.5us) passes after FET turns off, the latch operation is carried out being fitted with the upper condition and output switching is shut down. (Fig.16)

In the latch operation, Vcc voltage is maintained by the start-up circuit and the latch operation is maintained.

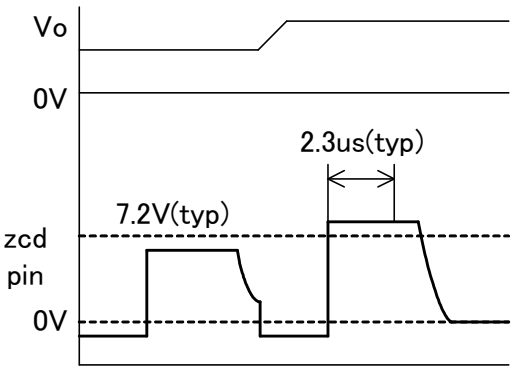


Fig.16 ZCD pin waveform for over-voltage on the secondary side

(2) No.2 pin (FB pin)

Function

(ｉ) Input of a feed-back signal from secondary error-amplifier.

(ii) Detection of an overload condition.

Usage

(ｉ) Input of a feedback signal

・Connection

This pin is connected with the receiver unit of a photo coupler. Concurrently it is connected a capacitor in parallel with the photo coupler to protect noise. (Fig. 17)

・Operation

This pin is biased by an IC internal power supply through a diode and a resistor.

The FB pin voltage is level-shifted and is input into a current comparator and finally gives the threshold voltage for MOSFET current signal that is detected on IS pin.

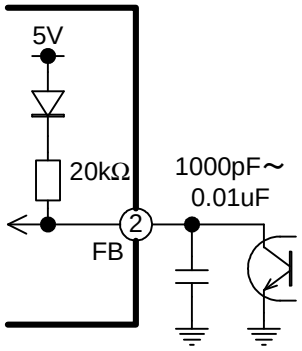


Fig.17 FB pin circuit

(ii) Detection of overload

・Connection

Same as (ｉ) Input of the feed back signal.

・Operation

If the output voltage of a power supply drops lower than the set value in an overload condition, FB pin voltage rises and scales out. This state is detected and judged as an overload condition. The threshold voltage to detect an overload is 3.5V (typ).

・Complement

FA5571/71A/73/70/5671 operates intermittently in an overload condition and auto restart if the overload condition is removed. Refer to pages 20 for detail operation.

FA5572/74 stops switching in an overload condition and goes into latch mode to maintain this condition. Refer to page 21 for detail operation.

(3) No.3 pin (IS pin)

Function

(**i**) Detection of MOSFET current

(**ii**) Difficulty for a burst operation at light load

(FA5571/71A/72/70/5671)

(**iii**) fsw reduction adjustment (FA5573/74)

(**iv**) Detection of transformer short circuit protection

Usage

(i) Current detection

・Connection

Connect a current detecting resistor Rs between a source pin of MOSFET and GNC. Input The current signal that arises in the MOSFET is input to this resistor (Fig.18).

・Operation

A MOSFET current signal that is input into IS pin is input into a current comparator. When it gets to the threshold voltage that is designated by FB pin, it turns off MOSFET. The maximum threshold voltage is 1V (typ.). MOSFET current is restricted by the current that corresponds to this voltage (1V) even in a transient condition at the startup or in an abnormal condition at overload

(ii) Burst operation adjustment (for FA5571/71A/72/70/5671)

・Connection

A resistor RIS is inserted additionally between the current detecting resistor Rs and IS pin (Fig. 19).

・Operation

A 50μA current supply is included in IS pin of FA5571/71A/72/70/5671, and electric current is sent out from IS pin. The voltage that is equal to the multiplication of the current value and the resistor value is effective to restrain burst operation.

・Compliment

For example, when getting into burst operation in case of a heavy load, the output ripple becomes bigger. If this is a problem, this pin should be used. However the more difficult it becomes to get into burst operation, the more electric power consumption in waiting increases.

(**iii**) fsw reduction adjustment

▪ Connection

Same as (**ii**) Burst operation adjustment

▪ Operation

FA5573/74 has 50μA internal current source inside IS pin and electric current flows out from IS pin. With the effect of the voltage resulting from the multiplication of this current value and the resistor Ris value, the frequency at light load has difficulty to lower.

▪ Compliment

For example, if switching frequency gets down to the audible frequency in waiting state and this is the problem, this method is used.

However, the more the difficulty to lower frequency increases the more power consumption in waiting increases.

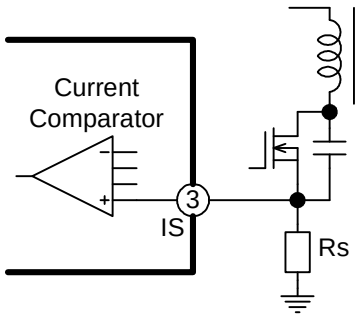


Fig.18 IS pin circuit

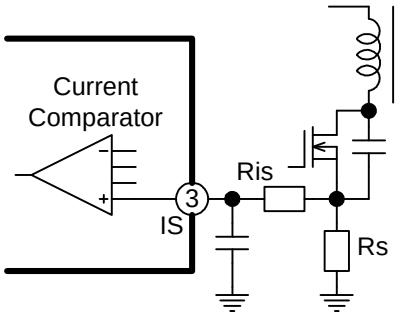


Fig.19 IS pin filter

(iv) Detection of transformer short circuit protection

- Connection

Same as (ii) Burst operation adjustment.

- Operation

If IS pin voltage exceeds 2.0V (typ.) due to the transformer short circuit and so on, FA5571/71A/72/73/74 causes latch stop.

(4) No.4 pin (GND pin)

Function

This is the standard voltage for each IC.

(5) No.5 pin (OUT pin)

Function

Driving of MOSFET.

Usage

- Connection

This pin is connected to MOSFET gate pin through a resistor (Fig.20, Fig.21, & Fig.22).

- Operation

During the period MOSFET is ON, this pin is kept in high position and almost the same voltage as Vcc is output.
During the period MOSFET is OFF, this pin is kept in low position and nearly zero voltage is output.

- Compliment

A gate resistor is connected to restrict current of OUT pin and to protect oscillation of gate pin voltage.
Output current rating of IC is 0.25A for source and 0.5A for sink.

(6) No.6 pin (VCC pin)

Function

(i) Provide power supply for IC

(ii) Detect over-voltage in primary side and activate latch protection. (FA5671)

Usage

(i) Provide power supply for IC

- Connection

Generally the auxiliary coil voltage of a transformer is rectified and smoothed and is connected to this pin. (Fig. 23)
In addition the auxiliary coil that is connected to ZCD pin can also be used for this pin.

- Operation

The voltage provided by the auxiliary coil should be set 11V to 28V(11V to 26V : FA5671) in normal operation.
It is possible to drive an IC with the current provided by the startup circuit without using an auxiliary coil, but standby power increases and heat dissipation of the IC also increases. Therefore it is better to provide Vcc from an auxiliary coil if lower standby power is required.
And also attention should be paid in selecting a MOSFET to drive because there is limitation of the current to be provided when it is driven only by the startup circuit.

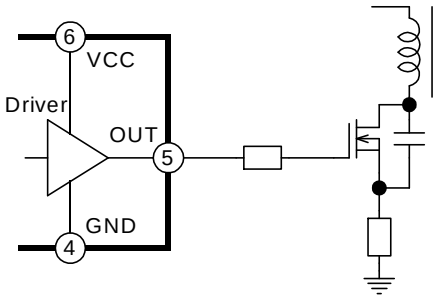


Fig.20 OUT pin circuit (1)

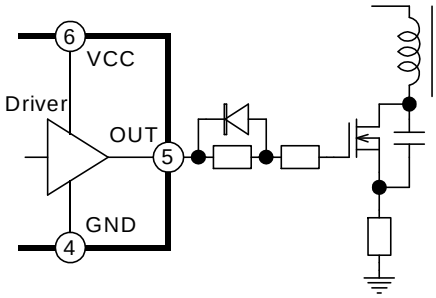


Fig.21 OUT pin circuit (2)

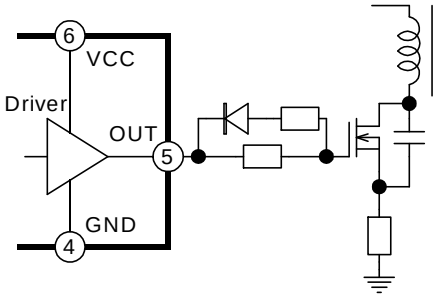


Fig.22 OUT pin circuit (3)

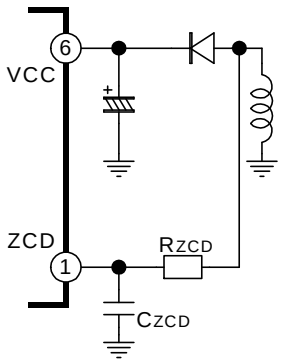


Fig.23 VCC circuit

(ii) Protection of over voltage (FA5671)

・Connection

Same as the connection described in (i)
Provision of power supply for IC.

・Operation

If Vcc exceeds 28V (typ.) and maintains more than 57μs (typ.), protection of over voltage is activated and IC is latched.

・Compliment

For example, if the output voltage rises abnormally due to the error of a feedback circuit, also Vcc rises abnormally. When Vcc exceeds 28V, latch protection is activated. Therefore that operates as over voltage protection of primary side detection.

(7) No.7 pin (N.C.)

As this pin is next to a high voltage pin, this pin is not yet connected to IC inside.

(8) No.8 pin (VH pin)

Function

Provides startup current.

Usage

・Connection

This pin is connected to a high voltage line. If this is connected after the current is rectified, this should be connected through a resistor of several kΩ (Fig.24). On the other hand, if connected before the current is rectified, this should be connected to a high voltage line through a resistor of several kΩ and a diode (Fig.25, Fig.26).

・Operation

If VH pin is connected to high voltage, current flows out from Vcc pin through the startup circuit in the IC. This current charges the capacitor between Vcc and GND, and Vcc voltage rises. When Vcc exceeds 18V (typ), IC is activated and begins to operate.

If Vcc is provided by an auxiliary winding, a startup circuit goes into shutdown state. On the other hand, if no power is supplied from the auxiliary winding, IC operates normally with a current provided by the startup circuit.

・Compliment

If Vcc is provided not by an auxiliary winding but only by a startup circuit, standby power requirement becomes larger and heat dissipation increases. Therefore it is better to provide Vcc by an auxiliary winding for low standby power dissipation requirement.

In addition, much attention is required in selecting MOSFET to drive, because there is a limit to the current to be provided when IC is driven only by a startup circuit.

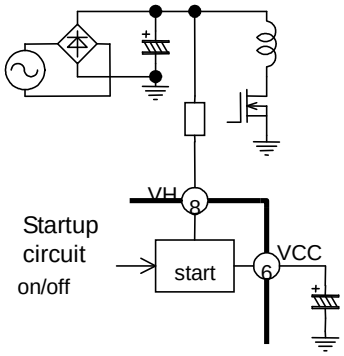


Fig.24 VH pin circuit (1)

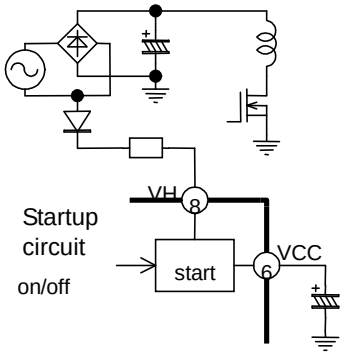


Fig.25 VH pin circuit (2)

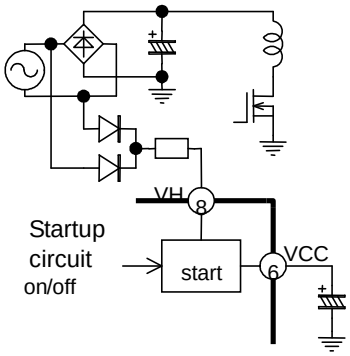


Fig.26 VH pin circuit (3)

11. Advice for designing

(1) Compensation for overload current detection

If the output of the power supply gets to the overload condition, the current to the MOSFET is limited by the maximum input threshold voltage of IS pin and the output voltage of the power supply drops down. If this condition continues, the current is shut down in the latch mode with overload protection function. (For the details of overload protection function, refer “9-(4) operation at overload”.)

At this time, the output current shut down in the latch mode varies according to the input voltage. In some case of shutdown in the latch mode, the higher the input voltage is, the bigger the output current becomes.

If this behavior is a problem, a resistor Ris should be connected between a current detection resistor Rs and IS pin and additionally a resistor R1 should be added for compensation. A resistor R1 is approximately several 100kΩ to several MegΩ depending on Ris.

Be careful that even if the input voltage is low with compensation, the output current of a power supply that is shut down in the latch mode is reduced a little.

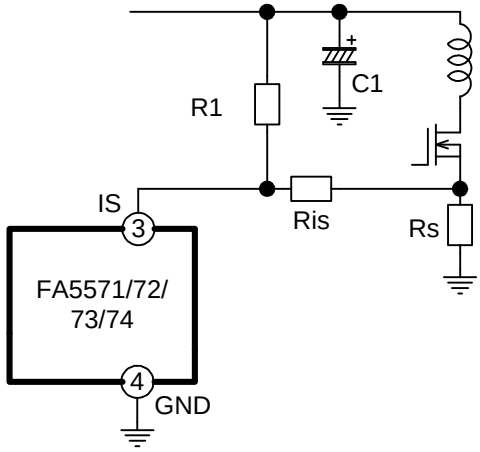


Fig.27 Compensation for overload protection

(2) Input power improvement at light load (FA5573/74)

FA5573/74 has a function in it that reduces the power loss by reducing oscillating frequency at light load.

But if reduction of the switching frequency is insufficient depending on a circuit being used, the power loss reduction at light load may be insufficient.

In such a case, a resistor R2 should be connected between an auxiliary coil and IS pin as shown in Fig.28. If Ris is 1kΩ, R2 is approximately several 100 kΩ to 1MegΩ. If R2 value is made smaller, the switching frequency can be decreased more at light load.

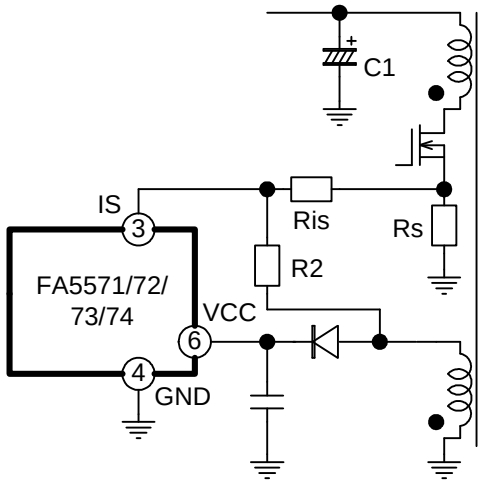


Fig.28 Compensation for input power improvement at light load

But during the MOSFET is ON, the minus voltage may be impressed to IS pin by R2 for a length of time. This minus voltage should not be lower than the absolute maximum rating, –0.3V.

In addition, if the switching frequency at light load is set too low, some noise in the transformer may be caused.

(3) Noise malfunction protection

This IC is an analog IC. Therefore if noise is impressed into each pin of this IC, malfunction may be caused. When any malfunction is detected, use the unit after checking fully of the power supply set by referring below. In addition, capacitors that are connected to each pin for noise protection should be connected nearest to the IC so as to operate effectively and also be careful about wiring layout.

(3-1) FB pin

FB pin provides the threshold voltage to a current comparator. If this pin is impressed noise, it causes disturbance of the output pulse. Usually a capacitor C2 is connected for noise protection as shown in Fig.29.

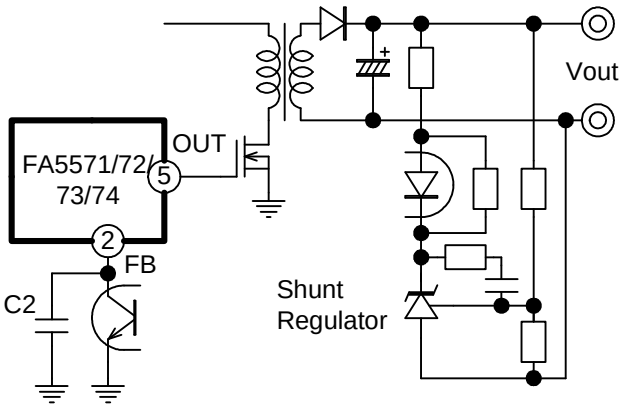


Fig.29 Noise malfunction protection (FB pin)

(3-2) IS pin

Since this IC has blanking function, it hardly causes the malfunction due to the surge current generated at turn-on of a MOSFET.

But if the surge current generated at turn-on is big or the noise other than turn-on is impressed from outside, the malfunction may occur.

In such a case, a CR filter should be added to IS pin as shown in Fig. 30.

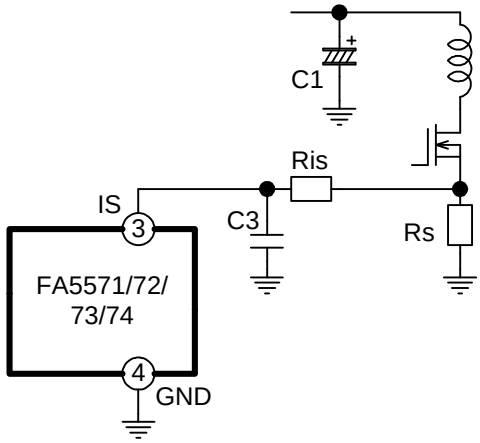


Fig.30 Noise malfunction protection (IS pin)

(3-3) VCC pin

Big current flows into VCC pin at the moment to drive a MOSFET and relatively big noise is easy to occur.

The current provided from an auxiliary coil also generates the noise.

If this noise is big, it may cause malfunction of IC. A decoupling capacitor C4 (over 0.1uF) should be added between VCC and GND in addition to an electrolytic condenser to reduce the noise generated in VCC pin as shown in Fig.31. C4 should be allocated nearest to VCC pin of the IC.

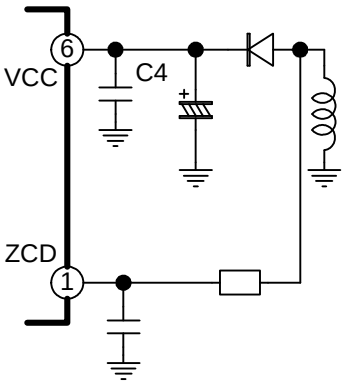


Fig.31 Noise malfunction protection (VCC pin)

(4) Malfunction protection due to the minus voltage on a pin

If the minus high voltage is impressed to each pin of an IC, a parasitic element in the IC works and may cause malfunction. The voltage impressed to each pin should be not higher than –0.3V.

If the voltage oscillation generated after MOSFET turns off is impressed on to OUT pin through a parasitic capacitor of a MOSFET, minus voltage may be impressed on to OUT pin. And also IS pin may be impressed minus voltage due to the current oscillation like surge generated at turn-off of a MOSFET.

In such a case a Schottky diode should be connected between each pin and GND. The forward voltage of a Schottky diode can prevent minus voltage of each pin. In this case a Schottky diode with the low forward voltage should be used. An example that a Schottky diode is connected to OUT pin is shown in Fig.32

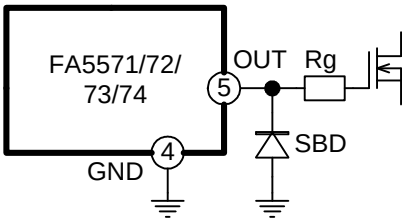


Fig.32 Minus voltage protection circuit

(5) Loss calculation

In order to use an IC within the rating, it is also necessary to calculate the loss of the IC. But it is difficult to measure the loss directly. Here an example of a rough calculation of the loss is shown.

The total loss Pd of an IC is roughly calculated in the following equation.

$Pd \approx Vcc \times (Iccop1 + Qg \times fsw) + V_{VH} \times IHrun$

Where, V_{VH} is the voltage impressed to VH pin, IHrun is the current flowing into VH pin in operation, Vcc is the voltage of power supply, Iccop1 is current consumption of an IC, Qg is the gate input electric charge of a MOSFET and fsw is the switching frequency.

The rough value of the total loss Pd is obtained by this equation and it is a little greater than the practical loss. In addition, it should be taken into account that each characteristic value has its variation and respective temperature characteristics.

Example)

If VH pin is connected to half-wave rectifier in case of AC 100V input, the average voltage impressed to VH pin is about 45V.

In this condition we suppose Vcc=15V, Qg=80nC and fsw=60kHz at Tj=25℃.

In case of FA5571, each value is as follows according to specific data. IHrun=30μA (typ.), Iccop1=1.35mA (typ.)

Then the typical loss of the IC is calculated as follows.

$Pd \approx 15V \times (1.35mA + 80nC \times 60kHz) + 45V \times 30\mu A$

$\approx 93.6mW$

(6) Protection of over-voltage on the secondary side

(FA5571/71A/72/73/74)

This IC can protect over-voltage on the secondary side with ZCD pin. The secondary over-voltage protection is performed as follows.

If the voltage of ZCD pin exceeds 7.2V (typ.) after 2.3μS (typ.) (71A : 4.5us) of turn-off of a FET, latch shutdown is carried out.

Rzcd that fixes the input threshold voltage of ZCD pin and Czcd that adjusts the resonance bottom point of Vds are connected to ZCD pin.

If these values of Rzcd and Czcd are not adequate, over-voltage protection may not operate normally. The waveform of ZCD pin at over-voltage protection is shown in Fig.34.

The waveform of ZCD pin in the upper part of Fig.34 shows that the voltage is normally detected at over-voltage on the secondary side and latch shutdown is carried out with the protection operation, but the lower waveform shows that as it does not exceed the threshold voltage for latch shutdown 2.3μS later, the protection operation is not carried out.

In such a case Rzcd and Czcd should be readjusted.

(7) Transformer short circuit protection with IS pin

(FA5571/71A/72/73/74)

This IC has function in it that carries out latch shutdown instantly when the voltage higher than 2V is impressed to IS pin to protect a transformer short circuit. This is shown in Fig.35.

This function also carries out instantly latch shutdown except a transformer short circuit when the voltage higher than 2V (typ.) is impressed to IS pin. Therefore if the high voltage is impressed to the input side such as lightning surge, the protection operation may carry out latch shutdown.

In such a case the values of IS pin filter Ris, C3 and a surge protection element for the input line should be readjusted.

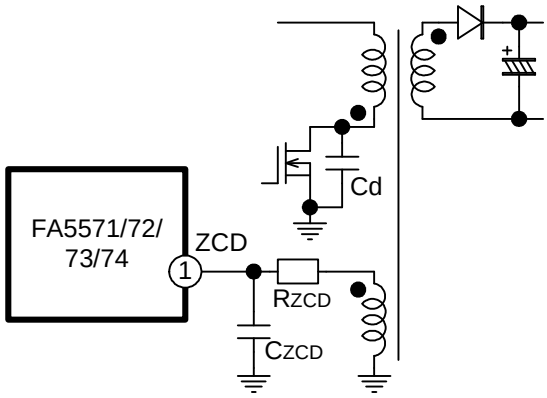


Fig.33 ZCD pin connection circuit

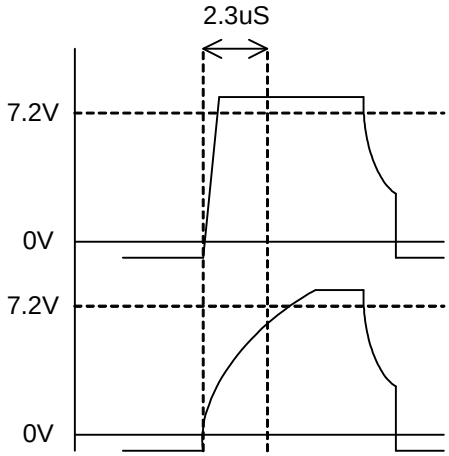


Fig.34 ZCD pin waveform at over-voltage

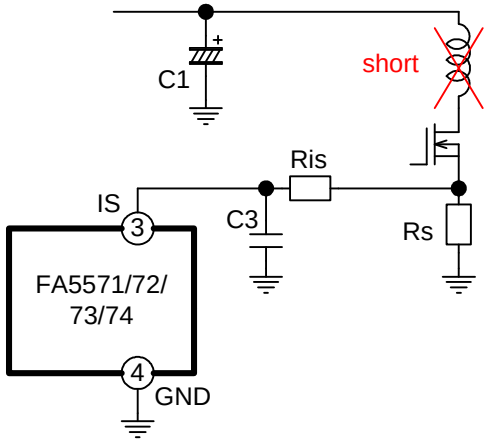


Fig.35 Transformer short circuit protection

12. Precautions for use

(1) Precautions for pattern design

In order to prevent the malfunction of the control IC (unstable voltage, unstable waveform, latch stop, etc.) caused by the surge voltage (noise) when a current is applied to the pattern on the minus side because of a principal current, a lightning surge test, an AC input surge test, and a static electricity test, consider the following contents when designing the pattern.

The power supply has the following current paths:

1) A principal current applied from the electrolytic capacitor to the primary winding of the transformer, the MOSFET, and the current sensing resistor after AC power supply rectification

2) A rectified current applied from the auxiliary winding of the transformer to the electrolytic capacitor; a drive current applied from the electrolytic capacitor to the control IC and the MOSFET gate.

3) A control current of the control IC for output feedback or the like

4) Filter and surge currents applied between the primary and secondary sides

▪ Separate the patterns on the minus side in 1) to 4) to avoid interference from each other.

▪ To reduce the surge voltage of the MOSFET, minimize the loop of the principal current path.

▪ Install the electrolytic and film capacitors between the VCC terminal and the GND in a closest position to each terminal in order to connect them at the shortest distance.

▪ Install the filter capacitors for the FB, IS, and ZCD terminals and the like in a closest position to each terminal in order to connect them at the shortest distance. Especially, separate the pattern on the minus side of the FB terminal from the other patterns if possible.

▪ Avoid installing the control circuit and pattern with high impedance directly below the transformer.

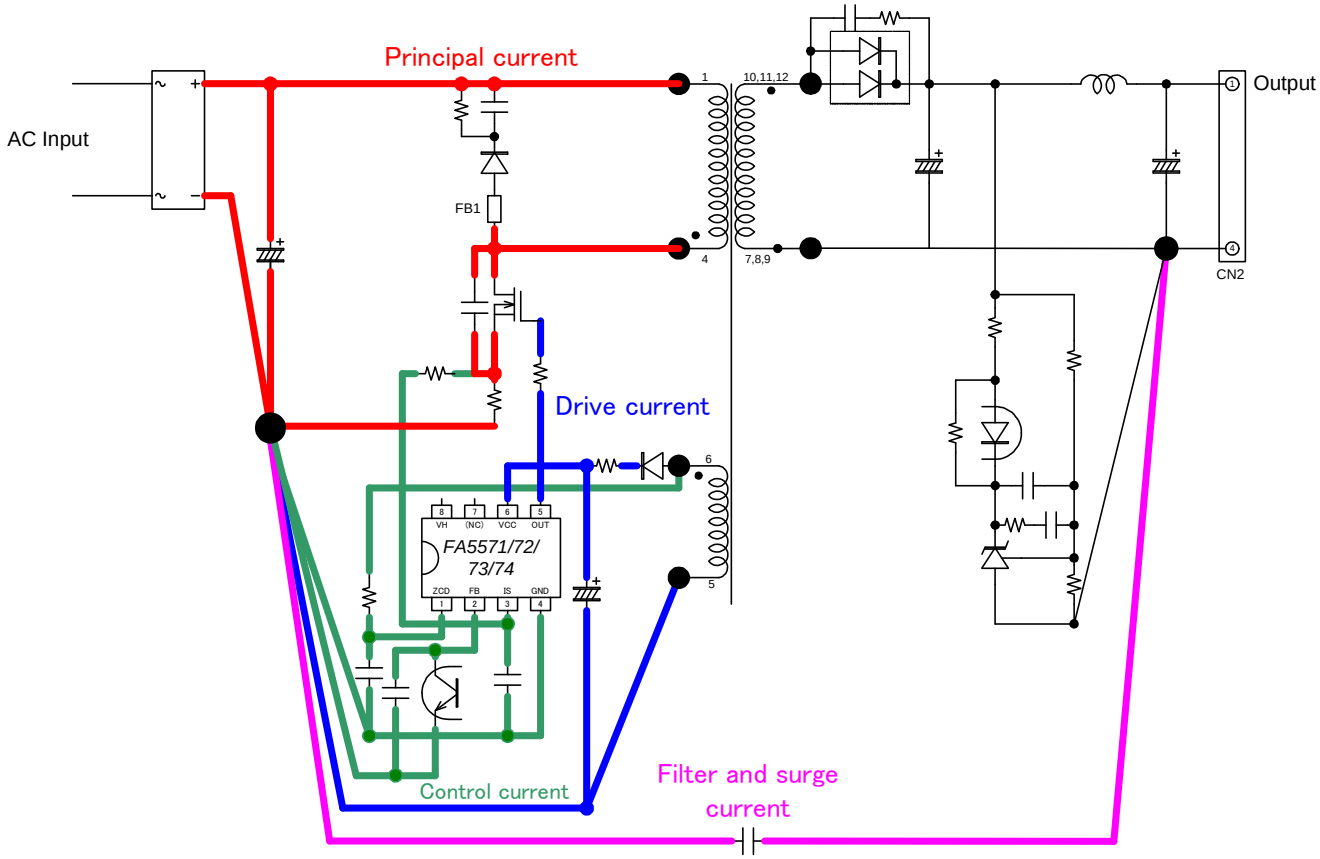


Fig.36 Pattern design image

(2) Latch stop in a surge test

The latch stop function of the IC has the following four modes:

1) Short-circuit protection function of the transformer

Latch stop immediately occurs if the IS terminal becomes 2.0 V or more because of short circuit of the transformer or the like.

2) Overvoltage protection function (FA5571/71A/72/73/74)

Latch stop is immediately caused if overvoltage occurs at the output on the secondary side and the ZCD terminal is 7.2 V or more when 2.3 us(71A：4.5us) passes after it is turned off because of the increased auxiliary winding voltage.

3) Latch function by an external signal

Latch stop occurs if the ZCD terminal is 7.2 V or more for 57 μs or more by an external signal or the like.

4) Overload protection function

Latch stop occurs if the FB terminal voltage is 3.5 V or more for 190 ms during overload.

(FA5571/71A/73/70/5671: auto restart, FA5572/74: latch)

Especially the latch stop functions in 1) and 2) above added for the FA5571 series may cause latch stop in noise tests such as a surge test. Any of the following adjustments can be performed as a measure in some cases:

(2-1) If the overvoltage protection function is estimated to have caused the latch stop

The latch by surge may be prevented if a capacitor C_{ZCD} with as much capacity as possible is attached to the ZCD terminal. Since the timing of the bottom detection when it is turned on is changed if the capacity of the capacitor C_{ZCD} is increased, reduce the resistance R_{ZCD} to adjust the time constant.

However, the overvoltage detection level is increased because of the reduced R_{ZCD}. As shown in fig. 37, add and connect resistor R1 in parallel with the IC built-in resistor to adjust the overvoltage detection level.

Since there is a possibility that this affects the standby electricity, check if it does.

(2-2) If the short-circuit protection function of the transformer is estimated to have caused the latch stop

The latch by surge may be prevented if increasing filter capacitor Cis of the IS terminal as much as possible. However, reduce the resistance Ris to adjust the time constant of the filter.

When the resistance Ris cannot be much increased because of the increased capacitor Cis, if it is intended to prevent the burst mode from being easily entered in particular, the adjustment cannot be performed.

In that case, as shown in fig. 38, add resistor R2 between the IS and VCC terminals to increase the IS terminal voltage in order to prevent the burst mode from being easily entered.

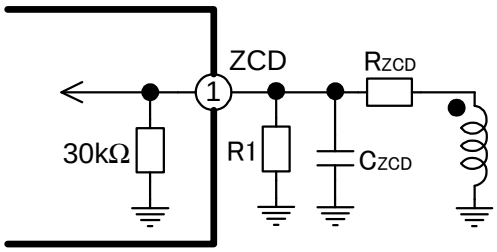


Fig. 37 Cause: overvoltage protection function

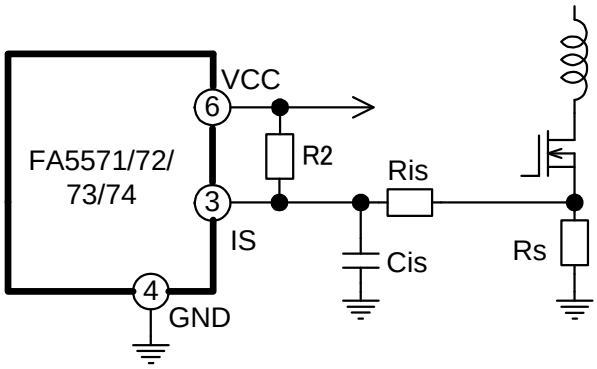


Fig. 38 Cause: short-circuit protection function of the transformer

(3) Abnormal sound of the transformer

1) Abnormal sound made by bottom skip operation

In the case of pseudo resonance, the lower the output load is, the higher the frequency is.

Since the maximum blanking frequency of this IC is 120 kHz(71A/5671：170kHz), if the frequency reaches 120 kHz, bottom skip operation is performed instead of continuous operation, limiting the frequency.

In the beginning after the frequency reaches 120 kHz, the bottom skip operation and the continuous operation are combined. The combined operation includes audio frequency and the transformer may make an abnormal sound.

In that case, when designing the transformer, reduce the minimum frequency at the maximum load as much as possible so that the bottom skip mode is entered at the lowest possible load.

2) Abnormal sound made by burst operation (FA5571/71A/72/70/5671)

▪ Moving the burst point

When burst operation starts at light load, if the frequency is in the audio range, the transformer may make an abnormal sound.

In this case, because increasing the resistance Ris in fig. 39 prevents the burst operation from being easily performed, the burst operation point can be moved to the light load side (see (ii) Burst operation adjustment on p. 25).

However, if increasing the resistance Ris, reduce Cis to prevent the CR time constant of the filter from being changed. Otherwise the burst operation may not be much changed.

▪ Changing the burst frequency

If the burst frequency is in the audio range, an abnormal sound may be made.

In this case, change the resistance R3 to change the photocoupler current in fig. 40 so that the burst frequency is changed.

However, when increasing the resistance and reducing the frequency, if increasing the resistance too much, the shunt REG cannot operate properly and the transient response performance of the output is deteriorated. Therefore, determine the operation after sufficient evaluation.

3) Abnormal sound made by decreased frequency (FA5573/FA5574)

If the frequency is reduced by the frequency reduction function at light load and the frequency is in the audio range, the transformer may make an abnormal sound.

In this case, change the frequency using the same method in 2) Abnormal sound made by burst operation (FA5571/71A/72/70/5671) for moving the burst point in order to identify the frequency for a smaller abnormal noise.

Larger resistance Ris prevents the frequency from being easily reduced and smaller resistance Ris makes it easier to reduce the frequency.

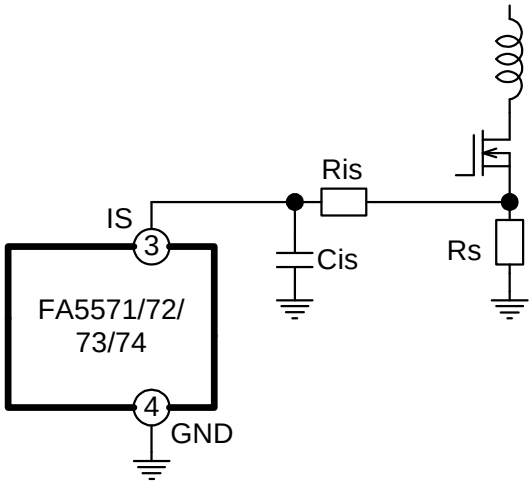


Fig. 39 Moving the burst point

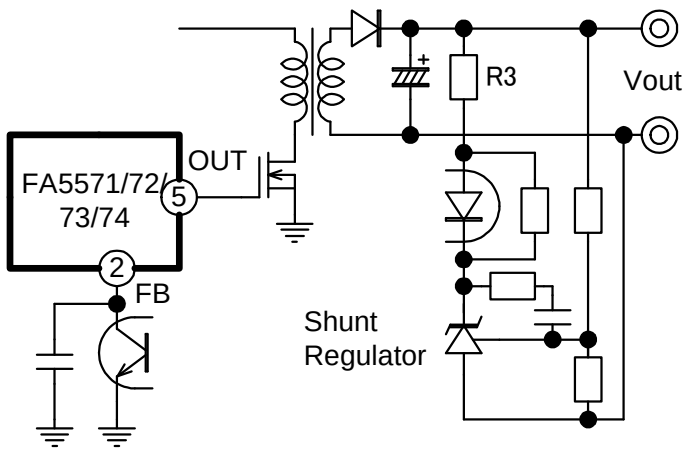
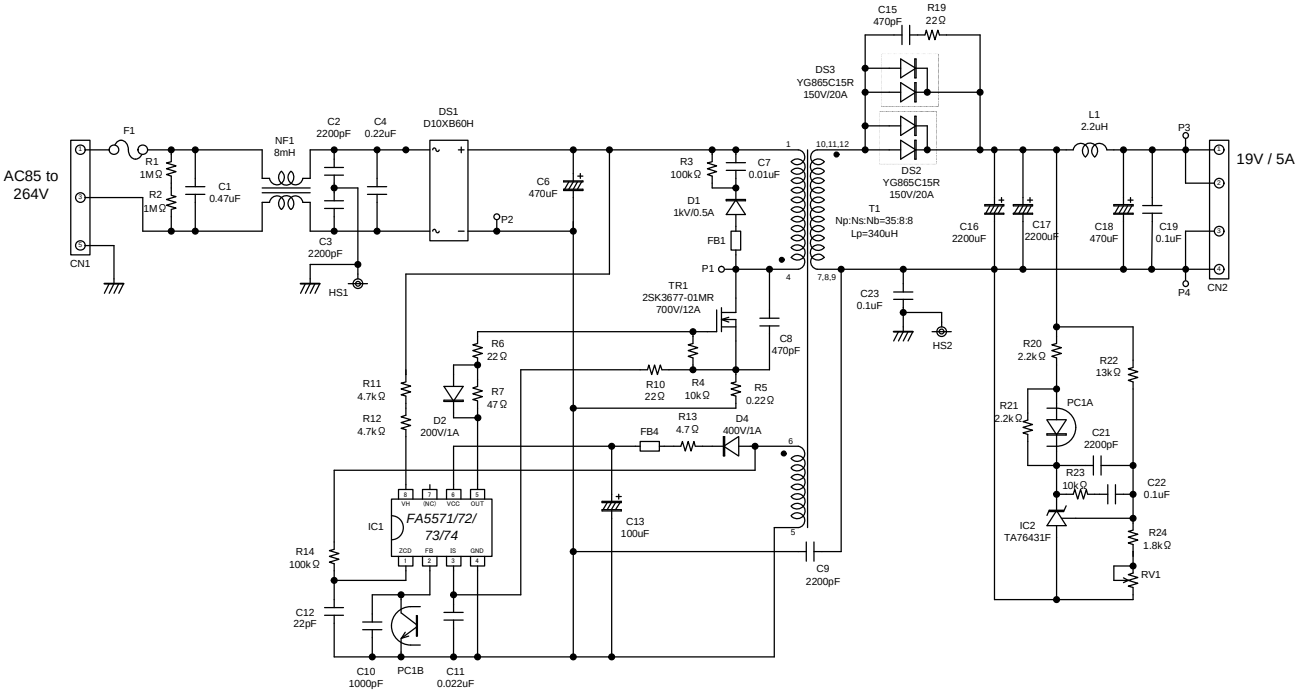


Fig. 40 Changing the burst frequency

13. Application circuit examples

These application examples show common specification for FA5571/71A/72/73/74/70/5671.

(1) Application circuit 1



(2) Application circuit 2

(To speed up latch reset after AC shutdown, VH pin (No.8) for start-up is connected to AC side.)